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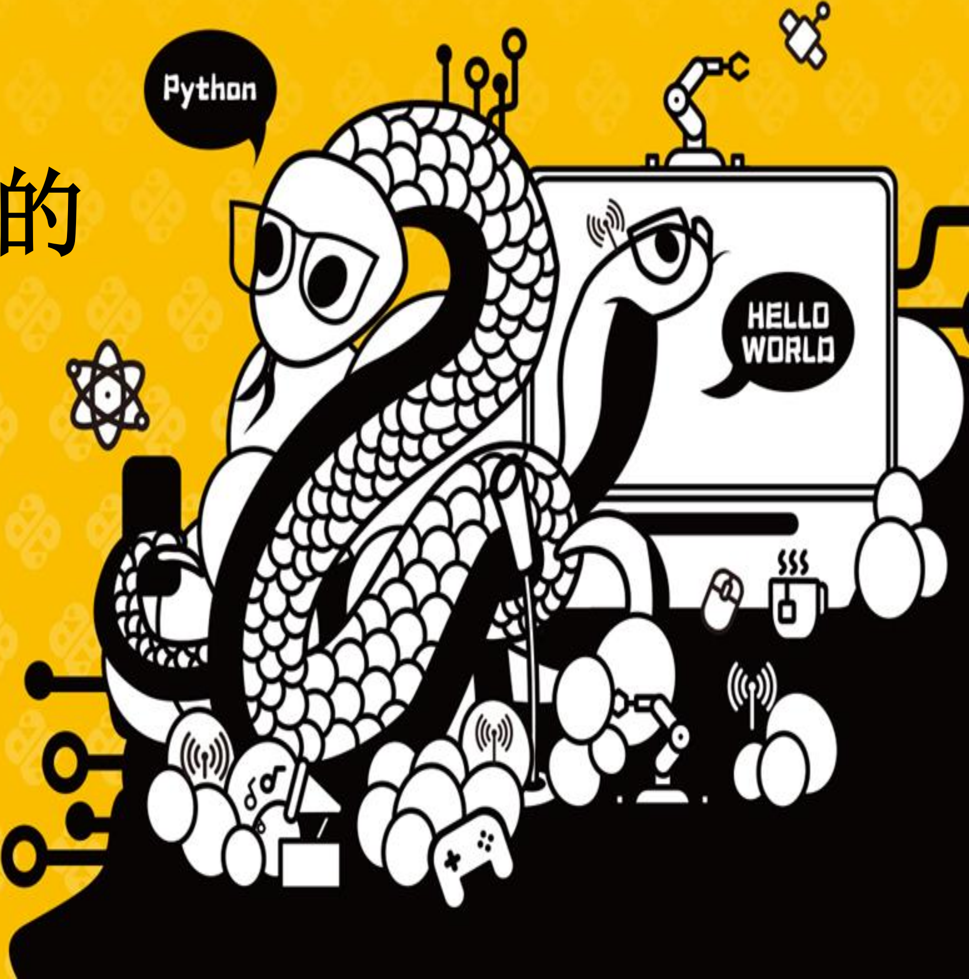
cocotb—硬件验证中的瑞士军刀

主讲人： 李枫 – 独立开发者



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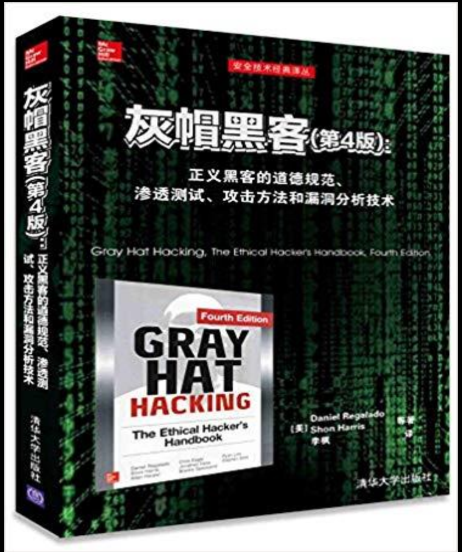
Who Am I

- An indie developer from China
- The main translator of the book «Gray Hat Hacking The Ethical Hacker's Handbook, Fourth Edition» (ISBN：9787302428671) & «Linux Hardening in Hostile Networks, First Edition» (ISBN: 9787115544384)


灰帽黑客(第4版):
正义黑客的道德规范、渗透测试、攻击方法和漏洞分析技术
Gray Hat Hacking, The Ethical Hackers Handbook, Fourth Edition
Fourth Edition
GRAY HAT HACKING
The Ethical Hacker's Handbook
清华大学出版社

- Pure software developmement for ~15 years(~11 years on Mobile dev)
- Actively participating Open Source Communities
- https://github.com/XianBeiTuoBaFeng2015/MySlides
- Recently, focus on infrastructure of Cloud/Edge Computing, AI, IoT, Programming Languages & Runtimes, Network, Virtualization, RISC-V, EDA, 5G/6G…

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Agenda

I. Background
- Tech Stack
- Overview of Python-based HW Verification
- Testbed

II. SpinalHDL with Cocotb on ARM
- RPi4

III. Corundum with Cocotb on ARM
- RPi4

IV. Project CocotbD
- The future of HW Verification
- Why is D
- Cocotb with D

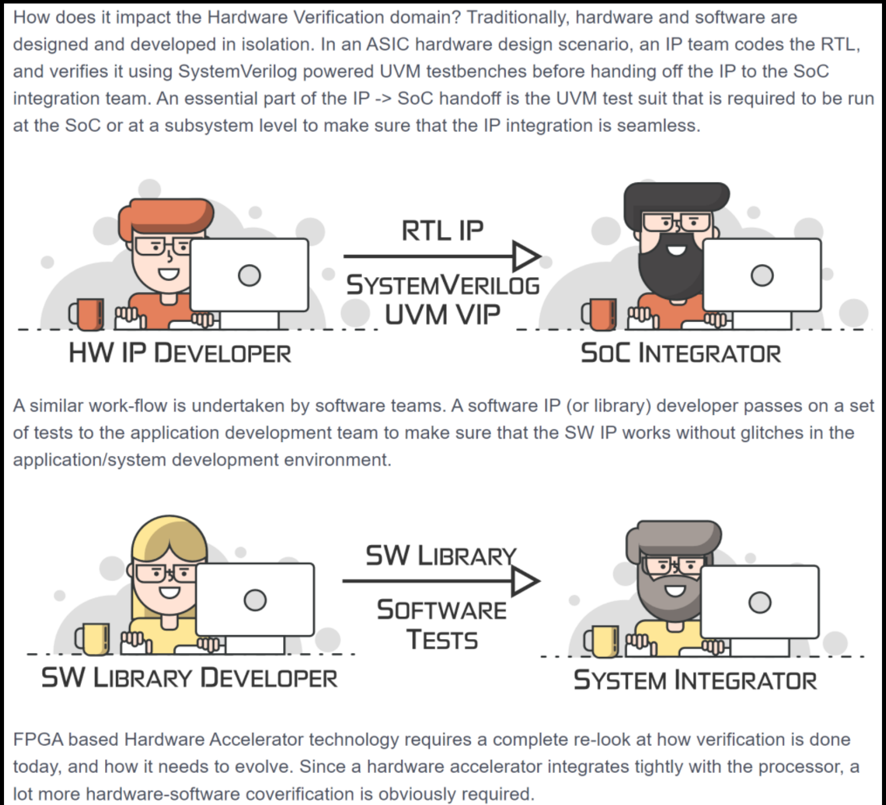
V. Wrap-up

I. Background

1) Tech Stack

1.1 HW Verification

What is it

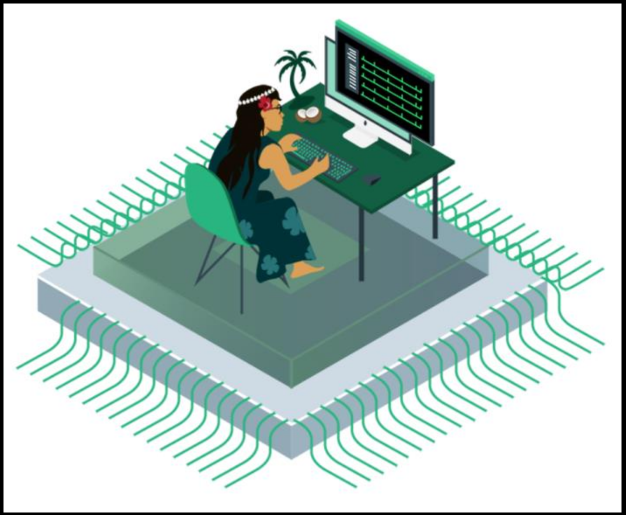
- 

How does it impact the Hardware Verification domain? Traditionally, hardware and software are designed and developed in isolation. In an ASIC hardware design scenario, an IP team codes the RTL, and verifies it using SystemVerilog powered UVM testbenches before handing off the IP to the SoC integration team. An essential part of the IP -> SoC handoff is the UVM test suit that is required to be run at the SoC or at a subsystem level to make sure that the IP integration is seamless.

A similar work-flow is undertaken by software teams. A software IP (or library) developer passes on a set of tests to the application development team to make sure that the SW IP works without glitches in the application/system development environment.

FPGA based Hardware Accelerator technology requires a complete re-look at how verification is done today, and how it needs to evolve. Since a hardware accelerator integrates tightly with the processor, a lot more hardware-software coverification is obviously required.

Source: http://uvm.io/blog/2019/04/accelerated-uvm/

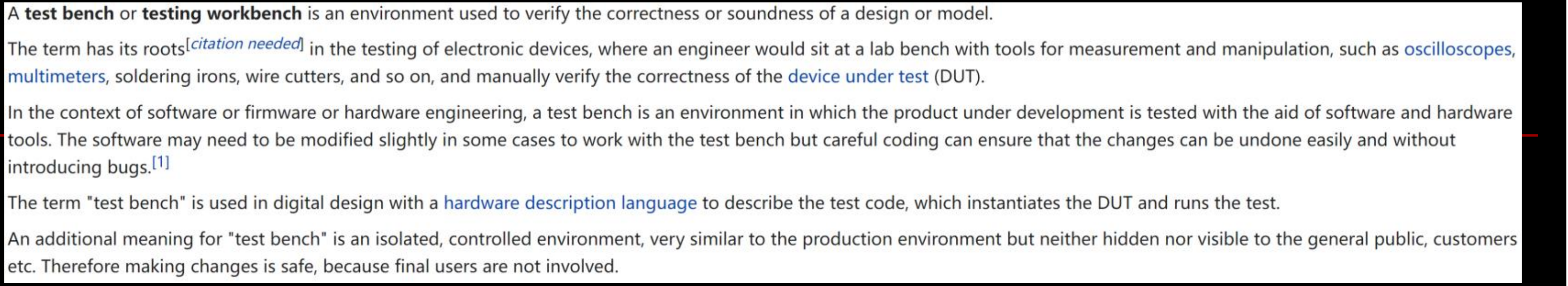


Source: https://www.cocotb.org/

- …

Terminologies

- https://en.wikipedia.org/wiki/Test_bench



A **test bench** or **testing workbench** is an environment used to verify the correctness or soundness of a design or model.

The term has its roots[citation needed] in the testing of electronic devices, where an engineer would sit at a lab bench with tools for measurement and manipulation, such as oscilloscopes, multimeters, soldering irons, wire cutters, and so on, and manually verify the correctness of the device under test (DUT).

In the context of software or firmware or hardware engineering, a test bench is an environment in which the product under development is tested with the aid of software and hardware tools. The software may need to be modified slightly in some cases to work with the test bench but careful coding can ensure that the changes can be undone easily and without introducing bugs.[1]

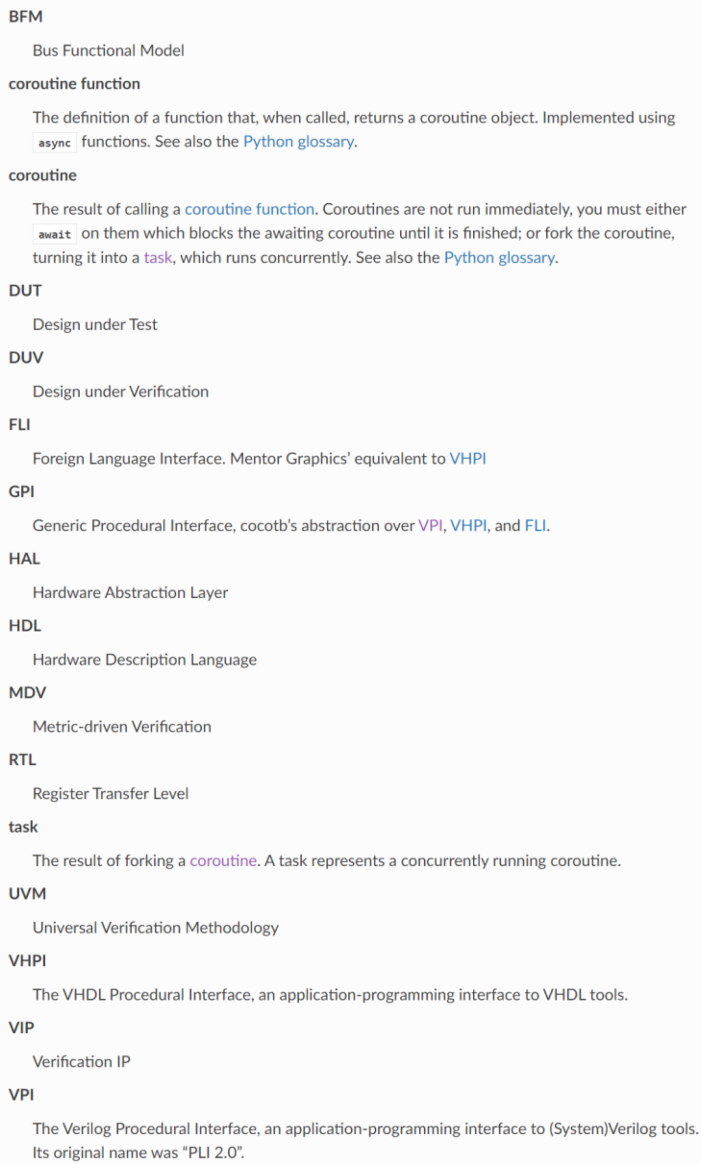
The term "test bench" is used in digital design with a hardware description language to describe the test code, which instantiates the DUT and runs the test.

An additional meaning for "test bench" is an isolated, controlled environment, very similar to the production environment but neither hidden nor visible to the general public, customers etc. Therefore making changes is safe, because final users are not involved.

- …

- …

- https://docs.cocotb.org/en/stable/glossary.html#term-VPI



BFM

Bus Functional Model

coroutine function

The definition of a function that, when called, returns a coroutine object. Implemented using `async` functions. See also the Python glossary.

coroutine

The result of calling a coroutine function. Coroutines are not run immediately, you must either `await` on them which blocks the awaiting coroutine until it is finished; or fork the coroutine, turning it into a task, which runs concurrently. See also the Python glossary.

DUT

Design under Test

DUV

Design under Verification

FLI

Foreign Language Interface. Mentor Graphics' equivalent to VHPI

GPI

Generic Procedural Interface, cocotb's abstraction over VPI, VHPI, and FLI.

HAL

Hardware Abstraction Layer

HDL

Hardware Description Language

MDV

Metric-driven Verification

RTL

Register Transfer Level

task

The result of forking a coroutine. A task represents a concurrently running coroutine.

UVM

Universal Verification Methodology

VHPI

The VHDL Procedural Interface, an application-programming interface to VHDL tools.

VIP

Verification IP

VPI

The Verilog Procedural Interface, an application-programming interface to (System)Verilog tools. Its original name was "PLI 2.0".

1.1.1 Languages

Hardware Description Language (HDL)

- https://en.wikipedia.org/wiki/Hardware_description_language
- https://en.wikipedia.org/wiki/Verilog
- …

Hardware Verification Language (HVL)

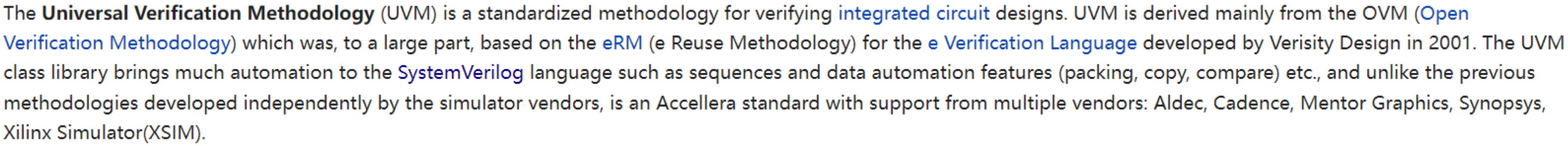
- https://en.wikipedia.org/wiki/Hardware_verification_language
- https://en.wikipedia.org/wiki/SystemVerilog
- …

1.1.2 Methodologies

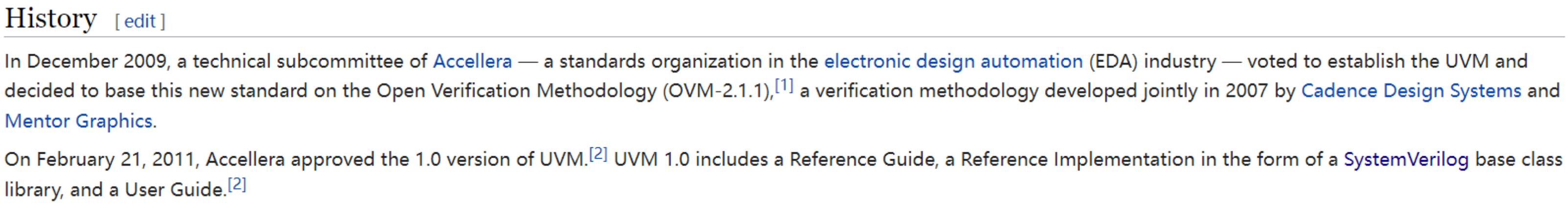
- https://github.com/ben-marshall/awesome-open-hardware-verification
- …

1.1.2.1 UVM

- https://en.wikipedia.org/wiki/Universal_Verification_Methodology



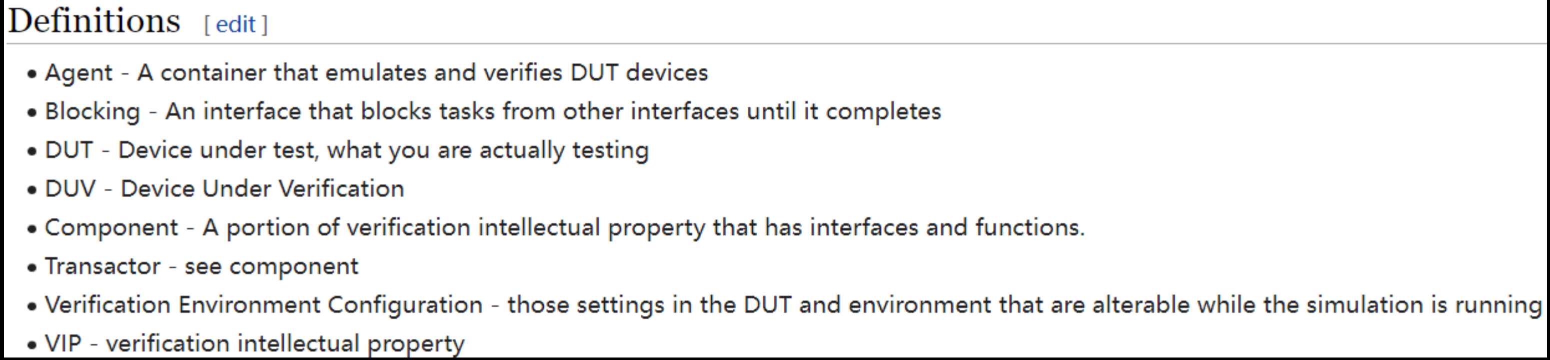
The **Universal Verification Methodology** (UVM) is a standardized methodology for verifying integrated circuit designs. UVM is derived mainly from the OVM (Open Verification Methodology) which was, to a large part, based on the eRM (e Reuse Methodology) for the e Verification Language developed by Verisity Design in 2001. The UVM class library brings much automation to the SystemVerilog language such as sequences and data automation features (packing, copy, compare) etc., and unlike the previous methodologies developed independently by the simulator vendors, is an Accellera standard with support from multiple vendors: Aldec, Cadence, Mentor Graphics, Synopsys, Xilinx Simulator(XSIM).



History [edit]

In December 2009, a technical subcommittee of Accellera — a standards organization in the electronic design automation (EDA) industry — voted to establish the UVM and decided to base this new standard on the Open Verification Methodology (OVM-2.1.1),[1] a verification methodology developed jointly in 2007 by Cadence Design Systems and Mentor Graphics.

On February 21, 2011, Accellera approved the 1.0 version of UVM.[2] UVM 1.0 includes a Reference Guide, a Reference Implementation in the form of a SystemVerilog base class library, and a User Guide.[2]



Definitions [edit]

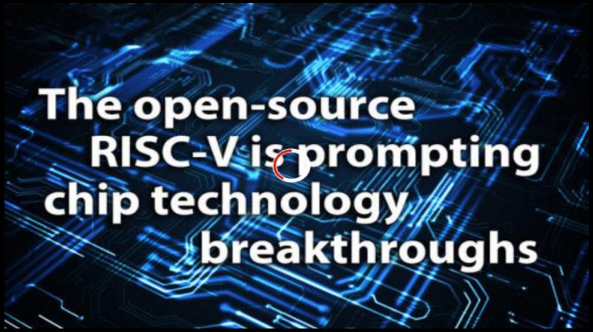
- Agent - A container that emulates and verifies DUT devices
- Blocking - An interface that blocks tasks from other interfaces until it completes
- DUT - Device under test, what you are actually testing
- DUV - Device Under Verification
- Component - A portion of verification intellectual property that has interfaces and functions.
- Transactor - see component
- Verification Environment Configuration - those settings in the DUT and environment that are alterable while the simulation is running
- VIP - verification intellectual property

…

- https://ieeexplore.ieee.org/document/9195920
- https://www.accellera.org/community/uvm/
- The latest version of UVM is 1.2, and 2.0 is on the way. https://www.accellera.org/downloads/standards/uvm
- …

1.2 FOSS EDA

- https://en.wikipedia.org/wiki/Comparison_of_EDA_software
- https://semiwiki.com/wikis/industry-wikis/eda-open-source-tools-wiki/
- https://fossi-foundation.org/
- ~~https://ieeexplore.ieee.org/document/9398963~~
- https://ieeexplore.ieee.org/document/9398960
- https://ieeexplore.ieee.org/document/9336682
- https://ieeexplore.ieee.org/document/9105619
- …



The Golden Age of Compilers

in an era of Hardware/Software co-design

International Conference on
Architectural Support for Programming Languages and
Operating Systems (ASPLOS 2021)

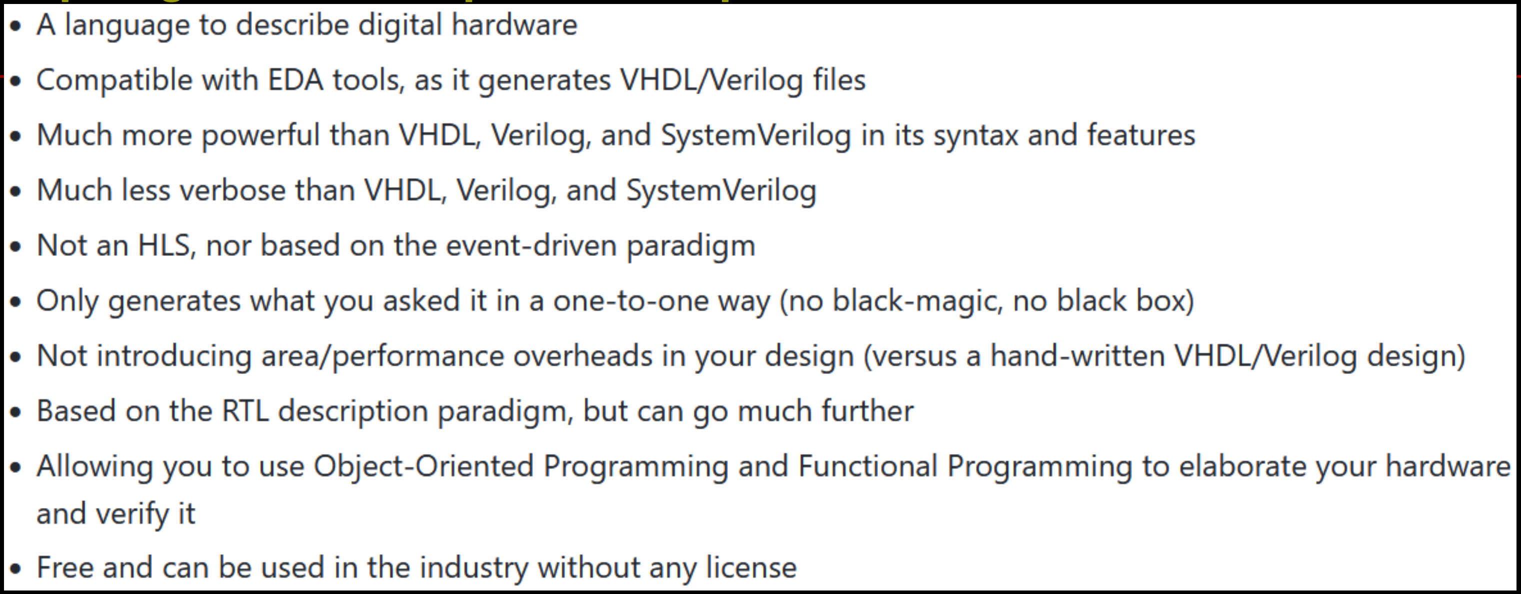
Chris Lattner
SiFive, Inc.

April 19, 2021

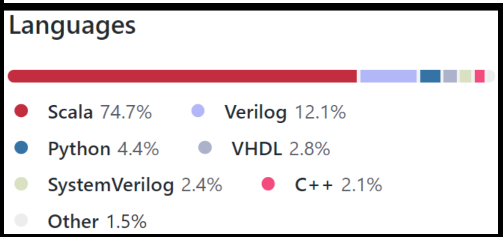
1.2.1 SpinalHDL

1.2.1.1 Overview

- https://github.com/SpinalHDL/SpinalHDL

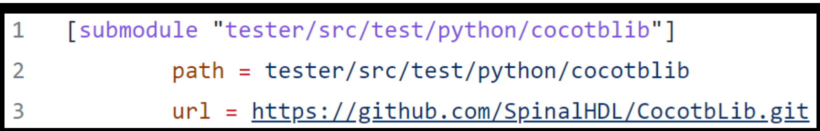


- A language to describe digital hardware
- Compatible with EDA tools, as it generates VHDL/Verilog files
- Much more powerful than VHDL, Verilog, and SystemVerilog in its syntax and features
- Much less verbose than VHDL, Verilog, and SystemVerilog
- Not an HLS, nor based on the event-driven paradigm
- Only generates what you asked it in a one-to-one way (no black-magic, no black box)
- Not introducing area/performance overheads in your design (versus a hand-written VHDL/Verilog design)
- Based on the RTL description paradigm, but can go much further
- Allowing you to use Object-Oriented Programming and Functional Programming to elaborate your hardware and verify it
- Free and can be used in the industry without any license



Languages

● Scala 74.7% ● Verilog 12.1%
● Python 4.4% ● VHDL 2.8%
● SystemVerilog 2.4% ● C++ 2.1%
● Other 1.5%

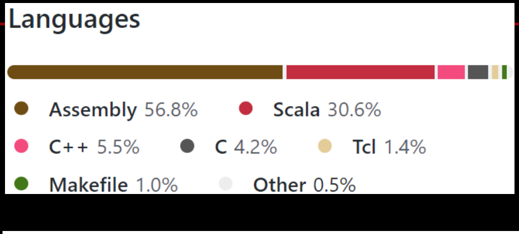


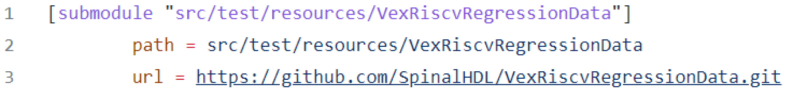
```
[submodule "tester/src/test/python/cocotblib"]
        path = tester/src/test/python/cocotblib
        url = https://github.com/SpinalHDL/CocotbLib.git
```

- https://spinalhdl.github.io/SpinalDoc-RTD/
- …

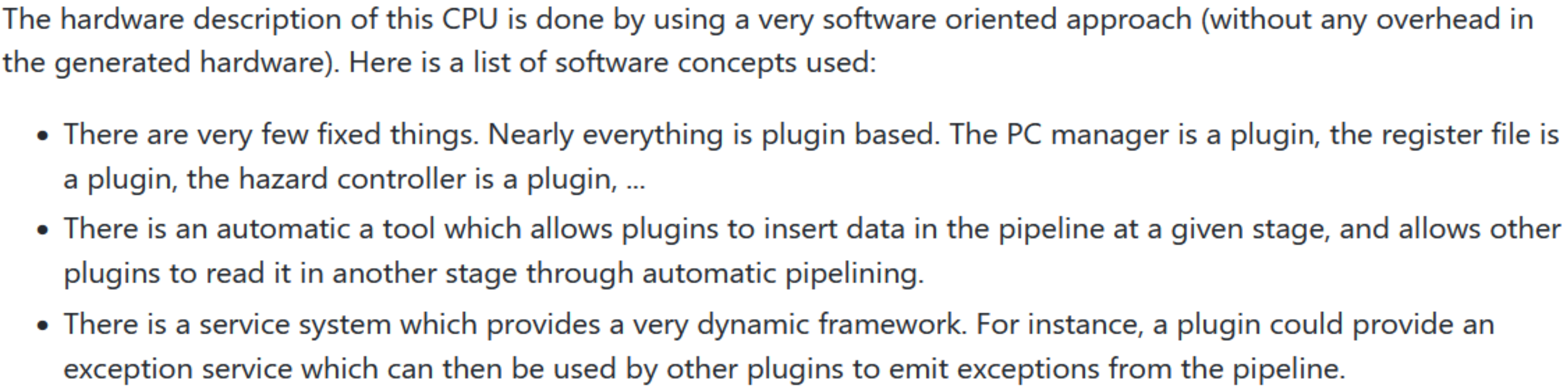
1.2.1.2 VexRiscv

- https://github.com/SpinalHDL/VexRiscv
  A FPGA friendly 32 bit RISC-V CPU implementation which is written in SpinalHDL.





```
[submodule "src/test/resources/VexRiscvRegressionData"]
	path = src/test/resources/VexRiscvRegressionData
	url = https://github.com/SpinalHDL/VexRiscvRegressionData.git
```

- 

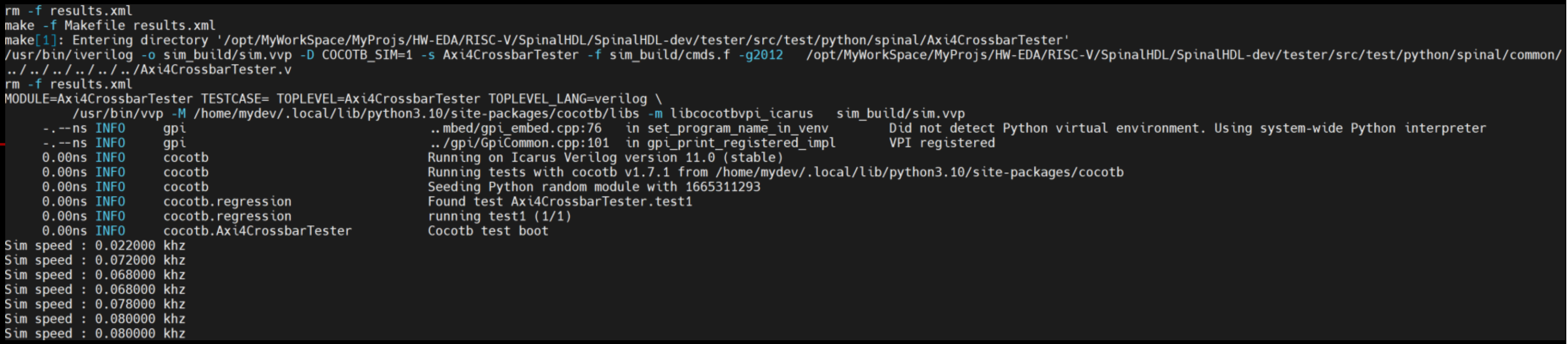
  The hardware description of this CPU is done by using a very software oriented approach (without any overhead in the generated hardware). Here is a list of software concepts used:

  - There are very few fixed things. Nearly everything is plugin based. The PC manager is a plugin, the register file is a plugin, the hazard controller is a plugin, ...
  - There is an automatic a tool which allows plugins to insert data in the pipeline at a given stage, and allows other plugins to read it in another stage through automatic pipelining.
  - There is a service system which provides a very dynamic framework. For instance, a plugin could provide an exception service which can then be used by other plugins to emit exceptions from the pipeline.

- https://riscv.org/announcements/2018/10/risc-v-contest/

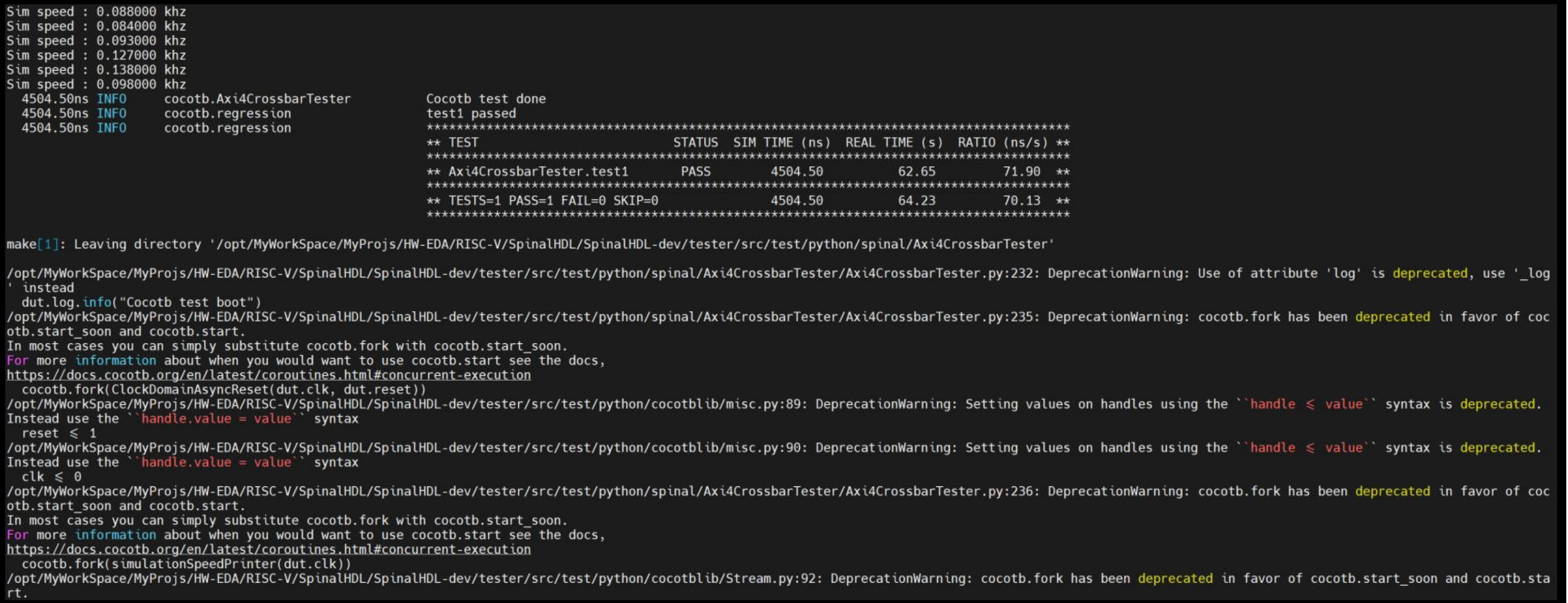
1.2.1.3 Cocotb in SpinalHDL

- ...



```
rm -f results.xml
make -f Makefile results.xml
make[1]: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester'
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s Axi4CrossbarTester -f sim_build/cmds.f -g2012   /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/common/
../../../../../../Axi4CrossbarTester.v
rm -f results.xml
MODULE=Axi4CrossbarTester TESTCASE= TOPLEVEL=Axi4CrossbarTester TOPLEVEL_LANG=verilog \
         /usr/bin/vvp -M /home/mydev/.local/lib/python3.10/site-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:76   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python interpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.7.1 from /home/mydev/.local/lib/python3.10/site-packages/cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1665311293
     0.00ns INFO     cocotb.regression                  Found test Axi4CrossbarTester.test1
     0.00ns INFO     cocotb.regression                  running test1 (1/1)
     0.00ns INFO     cocotb.Axi4CrossbarTester          Cocotb test boot
Sim speed : 0.022000 khz
Sim speed : 0.072000 khz
Sim speed : 0.068000 khz
Sim speed : 0.068000 khz
Sim speed : 0.078000 khz
Sim speed : 0.080000 khz
Sim speed : 0.080000 khz
```

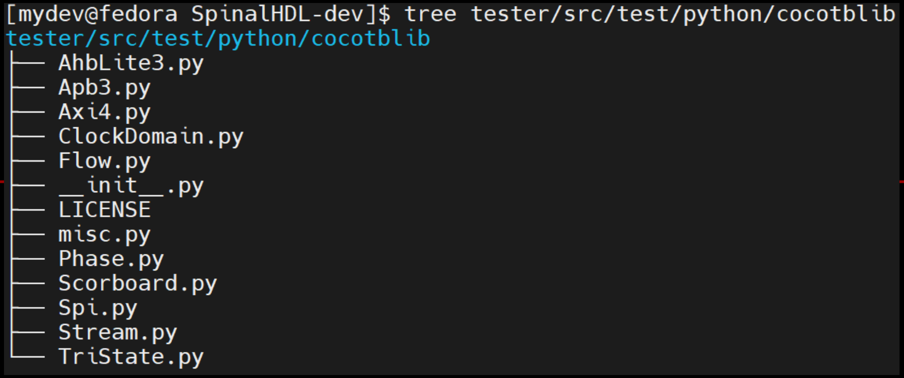
...



```
Sim speed : 0.088000 khz
Sim speed : 0.084000 khz
Sim speed : 0.093000 khz
Sim speed : 0.127000 khz
Sim speed : 0.138000 khz
Sim speed : 0.098000 khz
  4504.50ns INFO     cocotb.Axi4CrossbarTester          Cocotb test done
  4504.50ns INFO     cocotb.regression                  test1 passed
  4504.50ns INFO     cocotb.regression                  **************************************************************************************
                                                        ** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                        **************************************************************************************
                                                        ** Axi4CrossbarTester.test1       PASS        4504.50          62.65          71.90  **
                                                        **************************************************************************************
                                                        ** TESTS=1 PASS=1 FAIL=0 SKIP=0               4504.50          64.23          70.13  **
                                                        **************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester'

/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester/Axi4CrossbarTester.py:232: DeprecationWarning: Use of attribute 'log' is deprecated, use '_log
' instead
  dut.log.info("Cocotb test boot")
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester/Axi4CrossbarTester.py:235: DeprecationWarning: cocotb.fork has been deprecated in favor of coc
otb.start_soon and cocotb.start.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(ClockDomainAsyncReset(dut.clk, dut.reset))
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/misc.py:89: DeprecationWarning: Setting values on handles using the ``handle ≤ value`` syntax is deprecated.
Instead use the ``handle.value = value`` syntax
  reset ≤ 1
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/misc.py:90: DeprecationWarning: Setting values on handles using the ``handle ≤ value`` syntax is deprecated.
Instead use the ``handle.value = value`` syntax
  clk ≤ 0
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester/Axi4CrossbarTester.py:236: DeprecationWarning: cocotb.fork has been deprecated in favor of coc
otb.start_soon and cocotb.start.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(simulationSpeedPrinter(dut.clk))
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/Stream.py:92: DeprecationWarning: cocotb.fork has been deprecated in favor of cocotb.start_soon and cocotb.sta
rt.
```

...

cocotblib

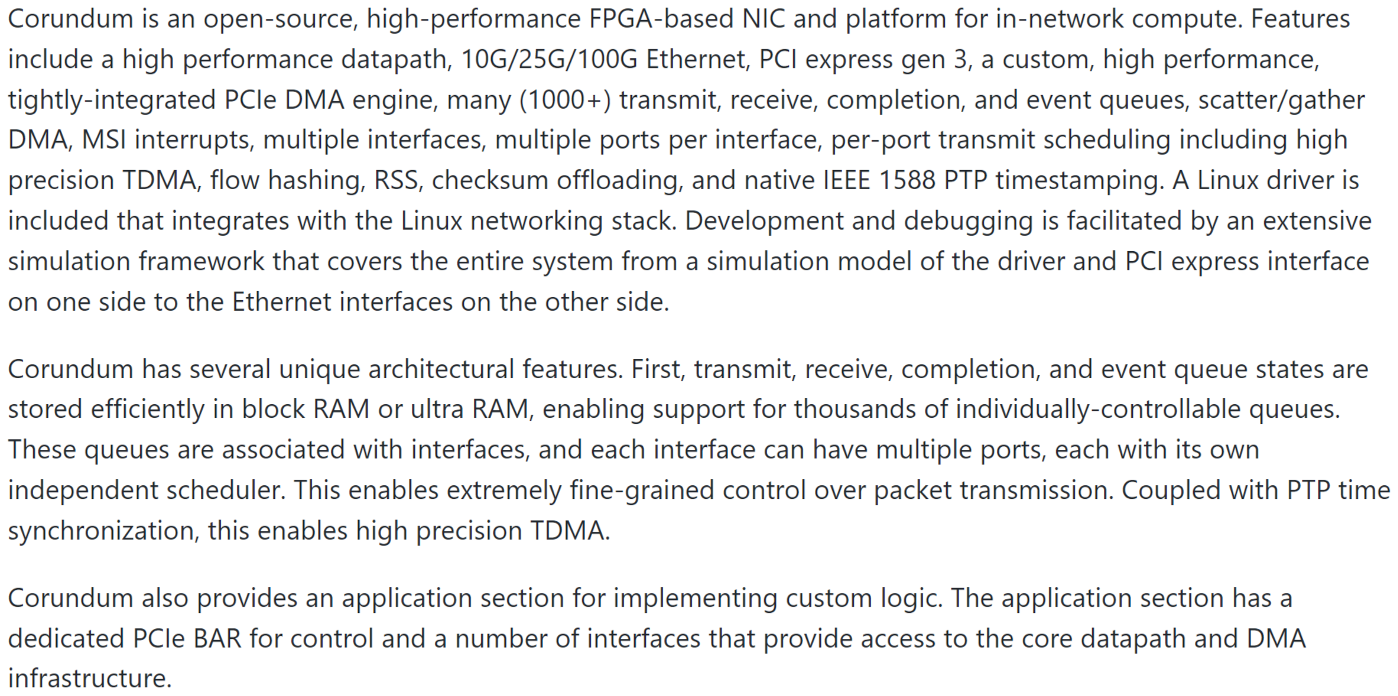


```
[mydev@fedora SpinalHDL-dev]$ tree tester/src/test/python/cocotblib
tester/src/test/python/cocotblib
├── AhbLite3.py
├── Apb3.py
├── Axi4.py
├── ClockDomain.py
├── Flow.py
├── __init__.py
├── LICENSE
├── misc.py
├── Phase.py
├── Scorboard.py
├── Spi.py
├── Stream.py
└── TriState.py
```

1.2.2 Corundum

1.2.2.1 Overview

- https://github.com/corundum/corundum/
  Open source FPGA-based NIC and platform for in-network compute.

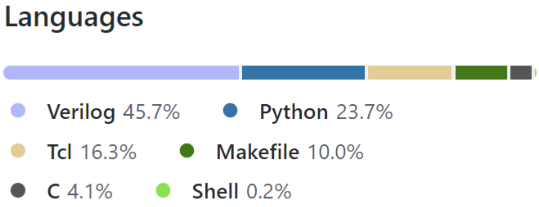


Corundum is an open-source, high-performance FPGA-based NIC and platform for in-network compute. Features include a high performance datapath, 10G/25G/100G Ethernet, PCI express gen 3, a custom, high performance, tightly-integrated PCIe DMA engine, many (1000+) transmit, receive, completion, and event queues, scatter/gather DMA, MSI interrupts, multiple interfaces, multiple ports per interface, per-port transmit scheduling including high precision TDMA, flow hashing, RSS, checksum offloading, and native IEEE 1588 PTP timestamping. A Linux driver is included that integrates with the Linux networking stack. Development and debugging is facilitated by an extensive simulation framework that covers the entire system from a simulation model of the driver and PCI express interface on one side to the Ethernet interfaces on the other side.

Corundum has several unique architectural features. First, transmit, receive, completion, and event queue states are stored efficiently in block RAM or ultra RAM, enabling support for thousands of individually-controllable queues. These queues are associated with interfaces, and each interface can have multiple ports, each with its own independent scheduler. This enables extremely fine-grained control over packet transmission. Coupled with PTP time synchronization, this enables high precision TDMA.

Corundum also provides an application section for implementing custom logic. The application section has a dedicated PCIe BAR for control and a number of interfaces that provide access to the core datapath and DMA infrastructure.

- **Src**



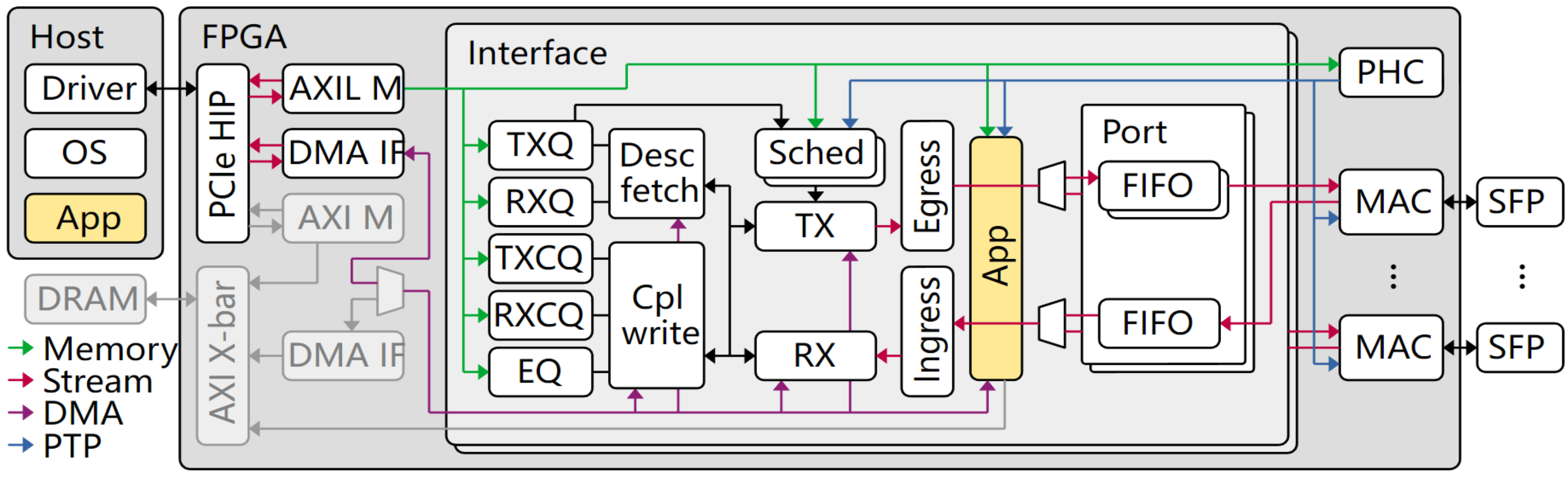
Languages

● Verilog 45.7% ● Python 23.7%
● Tcl 16.3% ● Makefile 10.0%
● C 4.1% ● Shell 0.2%

Contributors 9

Architecture & Design

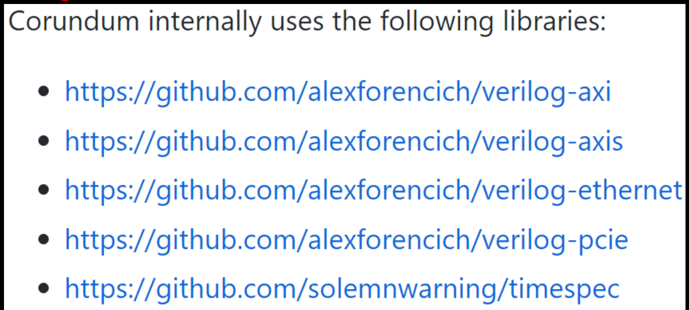
Block Diagram



Block diagram of the Corundum NIC. PCIe HIP: PCIe hard IP core; AXIL M: AXI lite master; DMA IF: DMA interface; AXI M: AXI master; PHC: PTP hardware clock; TXQ: transmit queue manager; TXCQ: transmit completion queue manager; RXQ: receive queue manager; RXCQ: receive completion queue manager; EQ: event queue manager; MAC + PHY: Ethernet media access controller (MAC) and physical interface layer (PHY).

Source: https://github.com/corundum/corundum/

Dependencies

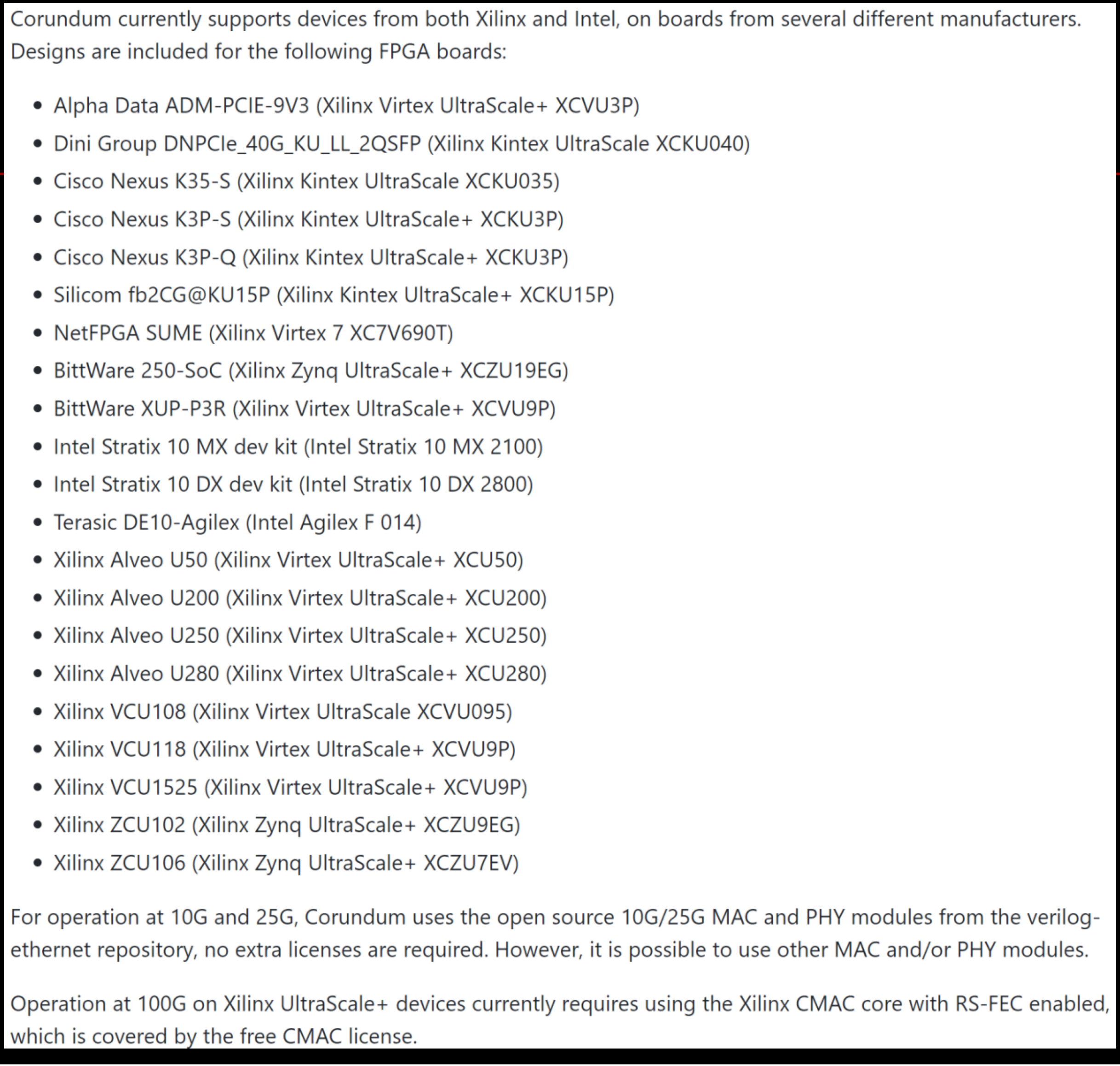


Corundum internally uses the following libraries:

- https://github.com/alexforencich/verilog-axi
- https://github.com/alexforencich/verilog-axis
- https://github.com/alexforencich/verilog-ethernet
- https://github.com/alexforencich/verilog-pcie
- https://github.com/solemnwarning/timespec

Source: https://github.com/corundum/corundum/

Supported boards



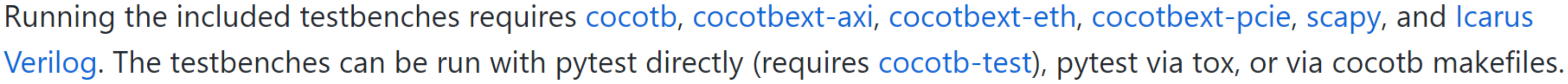
Corundum currently supports devices from both Xilinx and Intel, on boards from several different manufacturers. Designs are included for the following FPGA boards:

- Alpha Data ADM-PCIE-9V3 (Xilinx Virtex UltraScale+ XCVU3P)
- Dini Group DNPCIe_40G_KU_LL_2QSFP (Xilinx Kintex UltraScale XCKU040)
- Cisco Nexus K35-S (Xilinx Kintex UltraScale XCKU035)
- Cisco Nexus K3P-S (Xilinx Kintex UltraScale+ XCKU3P)
- Cisco Nexus K3P-Q (Xilinx Kintex UltraScale+ XCKU3P)
- Silicom fb2CG@KU15P (Xilinx Kintex UltraScale+ XCKU15P)
- NetFPGA SUME (Xilinx Virtex 7 XC7V690T)
- BittWare 250-SoC (Xilinx Zynq UltraScale+ XCZU19EG)
- BittWare XUP-P3R (Xilinx Virtex UltraScale+ XCVU9P)
- Intel Stratix 10 MX dev kit (Intel Stratix 10 MX 2100)
- Intel Stratix 10 DX dev kit (Intel Stratix 10 DX 2800)
- Terasic DE10-Agilex (Intel Agilex F 014)
- Xilinx Alveo U50 (Xilinx Virtex UltraScale+ XCU50)
- Xilinx Alveo U200 (Xilinx Virtex UltraScale+ XCU200)
- Xilinx Alveo U250 (Xilinx Virtex UltraScale+ XCU250)
- Xilinx Alveo U280 (Xilinx Virtex UltraScale+ XCU280)
- Xilinx VCU108 (Xilinx Virtex UltraScale XCVU095)
- Xilinx VCU118 (Xilinx Virtex UltraScale+ XCVU9P)
- Xilinx VCU1525 (Xilinx Virtex UltraScale+ XCVU9P)
- Xilinx ZCU102 (Xilinx Zynq UltraScale+ XCZU9EG)
- Xilinx ZCU106 (Xilinx Zynq UltraScale+ XCZU7EV)

For operation at 10G and 25G, Corundum uses the open source 10G/25G MAC and PHY modules from the verilog-ethernet repository, no extra licenses are required. However, it is possible to use other MAC and/or PHY modules.

Operation at 100G on Xilinx UltraScale+ devices currently requires using the Xilinx CMAC core with RS-FEC enabled, which is covered by the free CMAC license.

Testing

- 

  Running the included testbenches requires cocotb, cocotbext-axi, cocotbext-eth, cocotbext-pcie, scapy, and Icarus Verilog. The testbenches can be run with pytest directly (requires cocotb-test), pytest via tox, or via cocotb makefiles.

2) Overview of Python-based HW Verification

2.1 History

The oldest info?

- https://www.design-reuse.com/articles/15886/a-phyton-based-soc-validation-and-test-environment.html

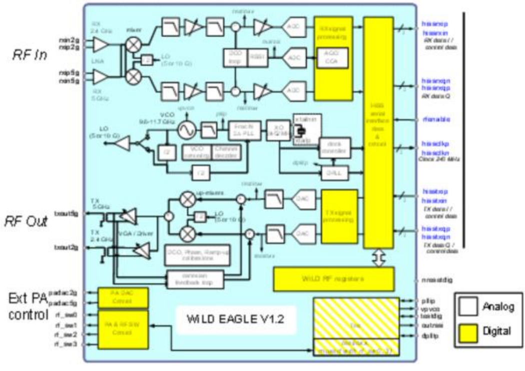


Figure 2: Eagle block diagram

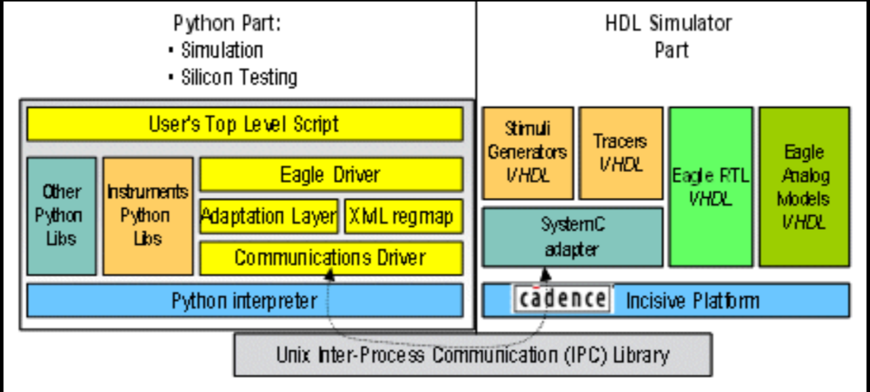


Figure 5: Software architecture (validation phase)

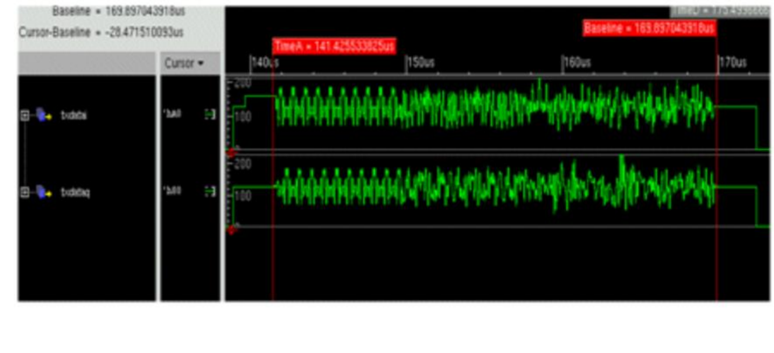

Baseline = 169.897043918us
Cursor-Baseline = -28.471510093us
Cursor
TimeA = 141.425533825us
Baseline = 169.897043918us
140us
150us
160us
170us

Figure 4: Testing reception: Python script and simulator output

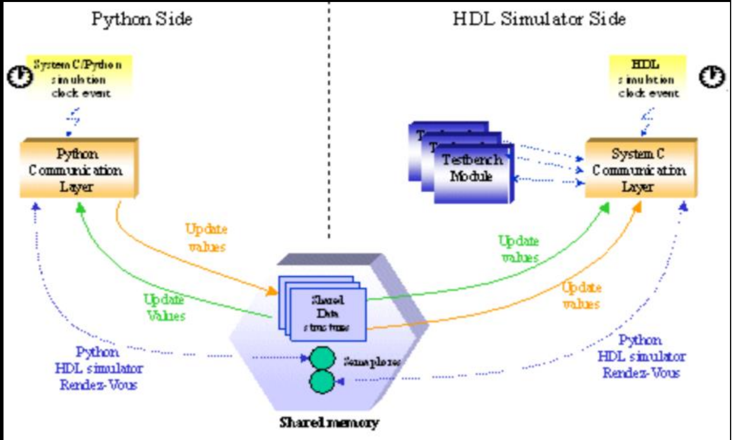

Python Side
HDL Simulator Side
System C/Python simulation clock event
HDL simulation clock event
Python Communication Layer
Testbench Module
System C Communication Layer
Update values
Update Values
Update values
Update values
Shared Data structures
Semaphores
Shared memory
Python HDL simulator Rendez-Vous
Python HDL simulator Rendez-Vous

Figure 6: Synchronization mechanism

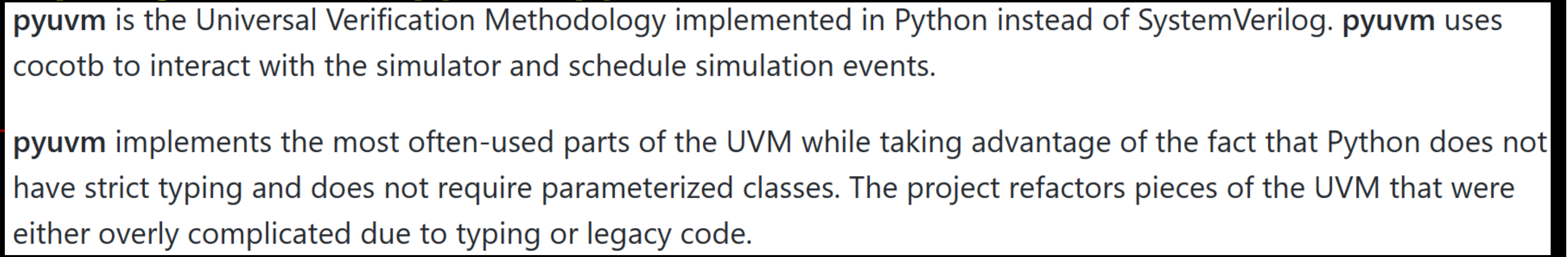
…

2.2 Python & UVM

- …

2.2.1 pyuvm

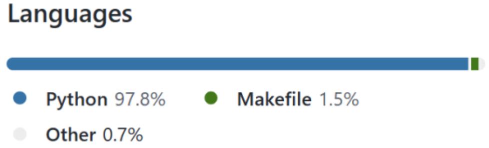
- https://github.com/pyuvm/pyuvm



pyuvm is the Universal Verification Methodology implemented in Python instead of SystemVerilog. **pyuvm** uses cocotb to interact with the simulator and schedule simulation events.

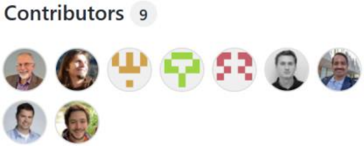
pyuvm implements the most often-used parts of the UVM while taking advantage of the fact that Python does not have strict typing and does not require parameterized classes. The project refactors pieces of the UVM that were either overly complicated due to typing or legacy code.

- Src



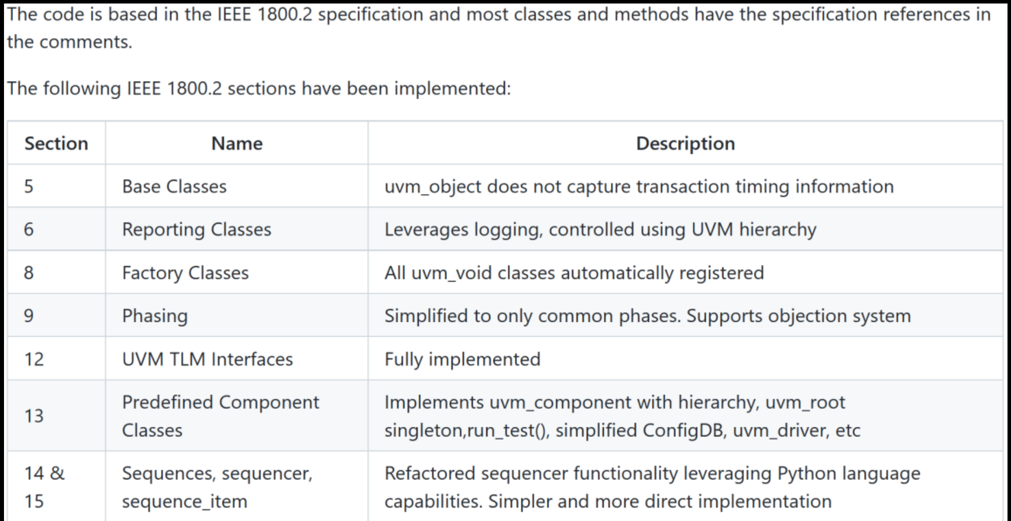
Languages

● Python 97.8% ● Makefile 1.5%
○ Other 0.7%



Contributors 9

- Current Status:



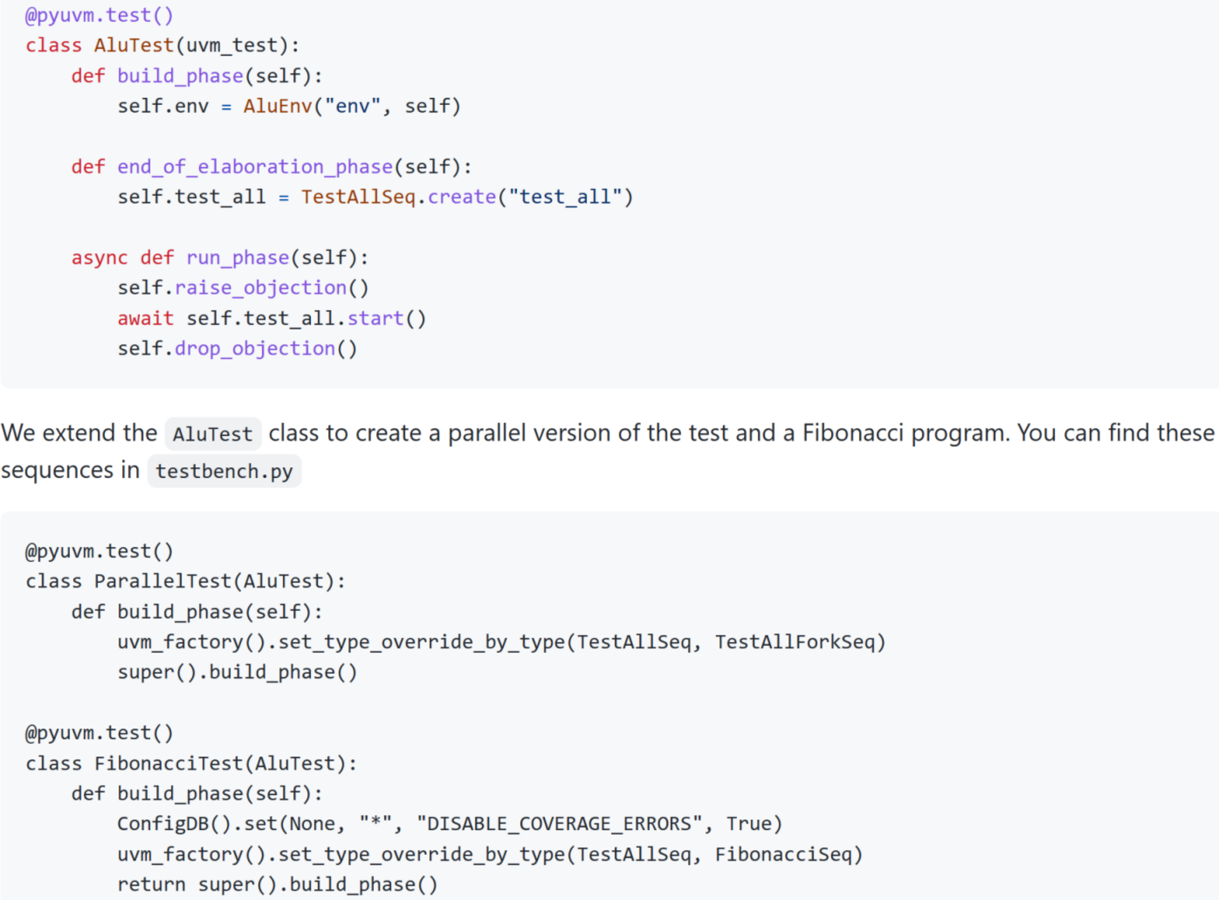
The code is based in the IEEE 1800.2 specification and most classes and methods have the specification references in the comments.

The following IEEE 1800.2 sections have been implemented:

Section	Name	Description
5	Base Classes	uvm_object does not capture transaction timing information
6	Reporting Classes	Leverages logging, controlled using UVM hierarchy
8	Factory Classes	All uvm_void classes automatically registered
9	Phasing	Simplified to only common phases. Supports objection system
12	UVM TLM Interfaces	Fully implemented
13	Predefined Component Classes	Implements uvm_component with hierarchy, uvm_root singleton,run_test(), simplified ConfigDB, uvm_driver, etc
14 & 15	Sequences, sequencer, sequence_item	Refactored sequencer functionality leveraging Python language capabilities. Simpler and more direct implementation

- https://verificationacademy.com/news/the-python-for-verification-series

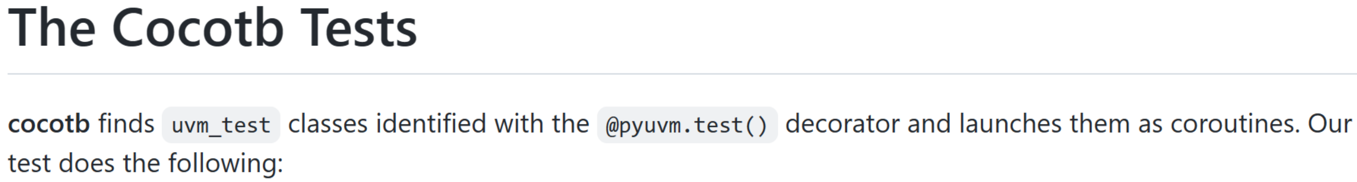
Tests



```
@pyuvm.test()
class AluTest(uvm_test):
    def build_phase(self):
        self.env = AluEnv("env", self)

    def end_of_elaboration_phase(self):
        self.test_all = TestAllSeq.create("test_all")

    async def run_phase(self):
        self.raise_objection()
        await self.test_all.start()
        self.drop_objection()
```

We extend the `AluTest` class to create a parallel version of the test and a Fibonacci program. You can find these sequences in `testbench.py`

```
@pyuvm.test()
class ParallelTest(AluTest):
    def build_phase(self):
        uvm_factory().set_type_override_by_type(TestAllSeq, TestAllForkSeq)
        super().build_phase()

@pyuvm.test()
class FibonacciTest(AluTest):
    def build_phase(self):
        ConfigDB().set(None, "*", "DISABLE_COVERAGE_ERRORS", True)
        uvm_factory().set_type_override_by_type(TestAllSeq, FibonacciSeq)
        return super().build_phase()
```



The Cocotb Tests

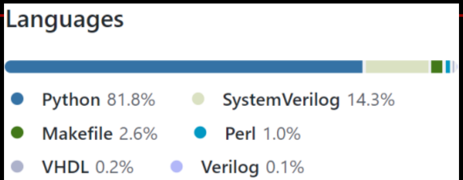
cocotb finds `uvm_test` classes identified with the `@pyuvm.test()` decorator and launches them as coroutines. Our test does the following:

...

2.2.2 UVM-Python

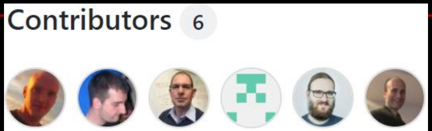
- https://github.com/tpoikela/uvm-python

  UVM 1.2 port to Python
- Src



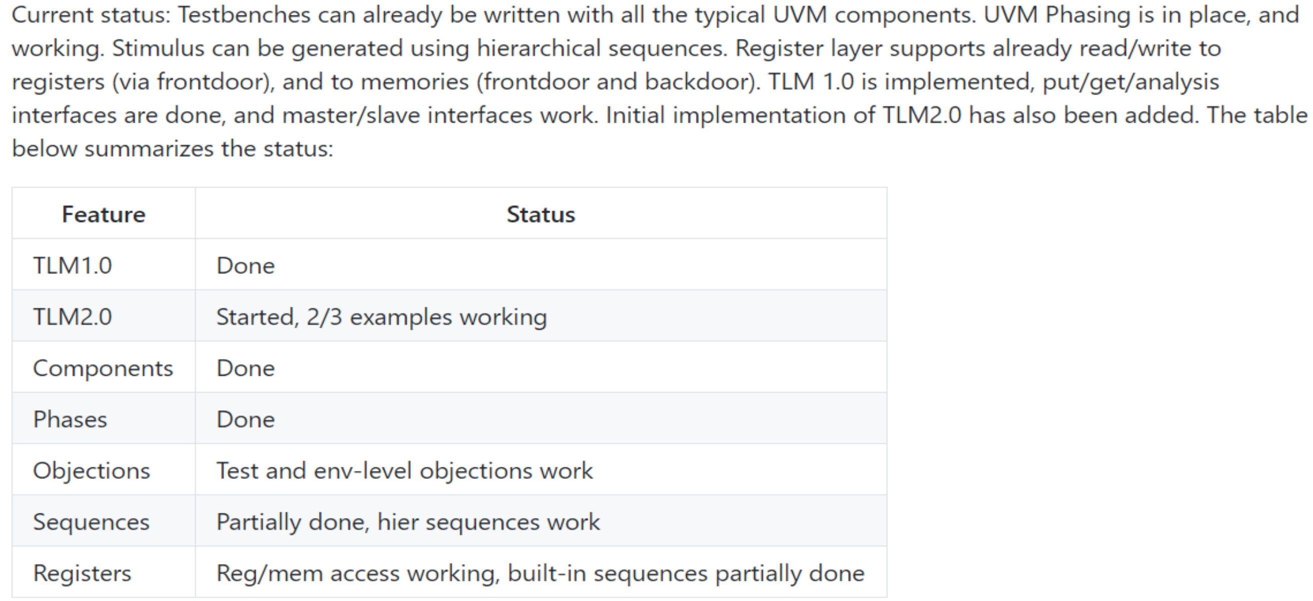
Languages

● Python 81.8% ● SystemVerilog 14.3%
● Makefile 2.6% ● Perl 1.0%
● VHDL 0.2% ● Verilog 0.1%



Contributors 6

- Current Status:



Current status: Testbenches can already be written with all the typical UVM components. UVM Phasing is in place, and working. Stimulus can be generated using hierarchical sequences. Register layer supports already read/write to registers (via frontdoor), and to memories (frontdoor and backdoor). TLM 1.0 is implemented, put/get/analysis interfaces are done, and master/slave interfaces work. Initial implementation of TLM2.0 has also been added. The table below summarizes the status:

Feature	Status
TLM1.0	Done
TLM2.0	Started, 2/3 examples working
Components	Done
Phases	Done
Objections	Test and env-level objections work
Sequences	Partially done, hier sequences work
Registers	Reg/mem access working, built-in sequences partially done

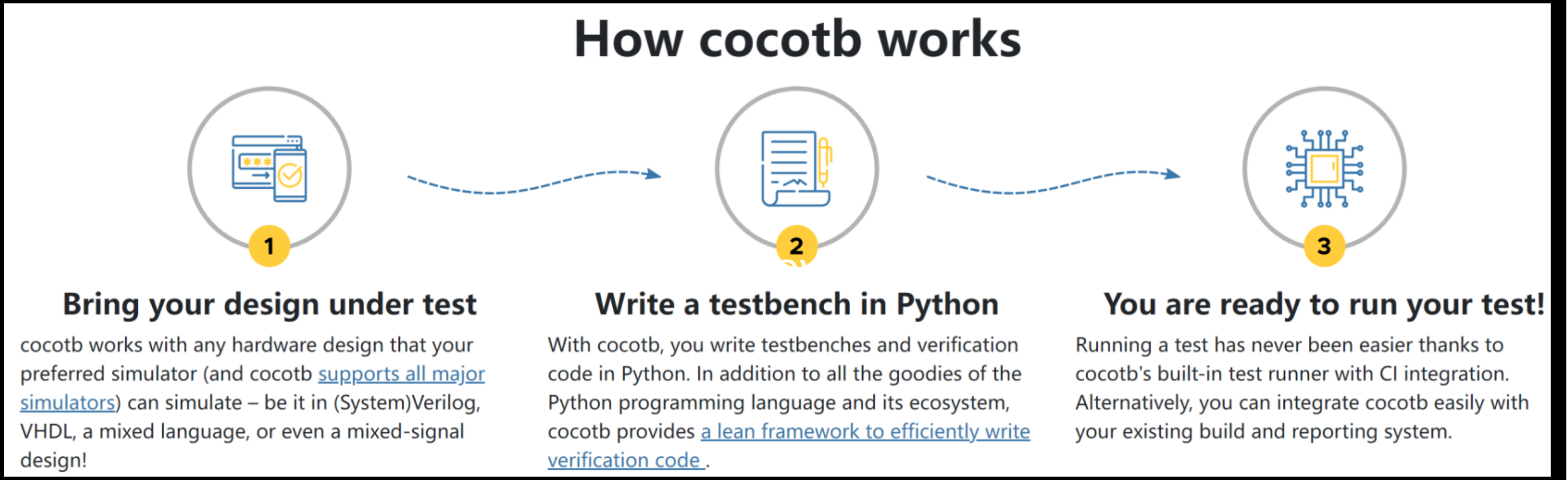
- …

2.3 Cocotb

2.3.1 Overview

- https://www.cocotb.org/

  A Coroutine based Cosimulation TestBench environment for verifying VHDL and Verilog RTL using Python.



How cocotb works

Bring your design under test

cocotb works with any hardware design that your preferred simulator (and cocotb supports all major simulators) can simulate – be it in (System)Verilog, VHDL, a mixed language, or even a mixed-signal design!

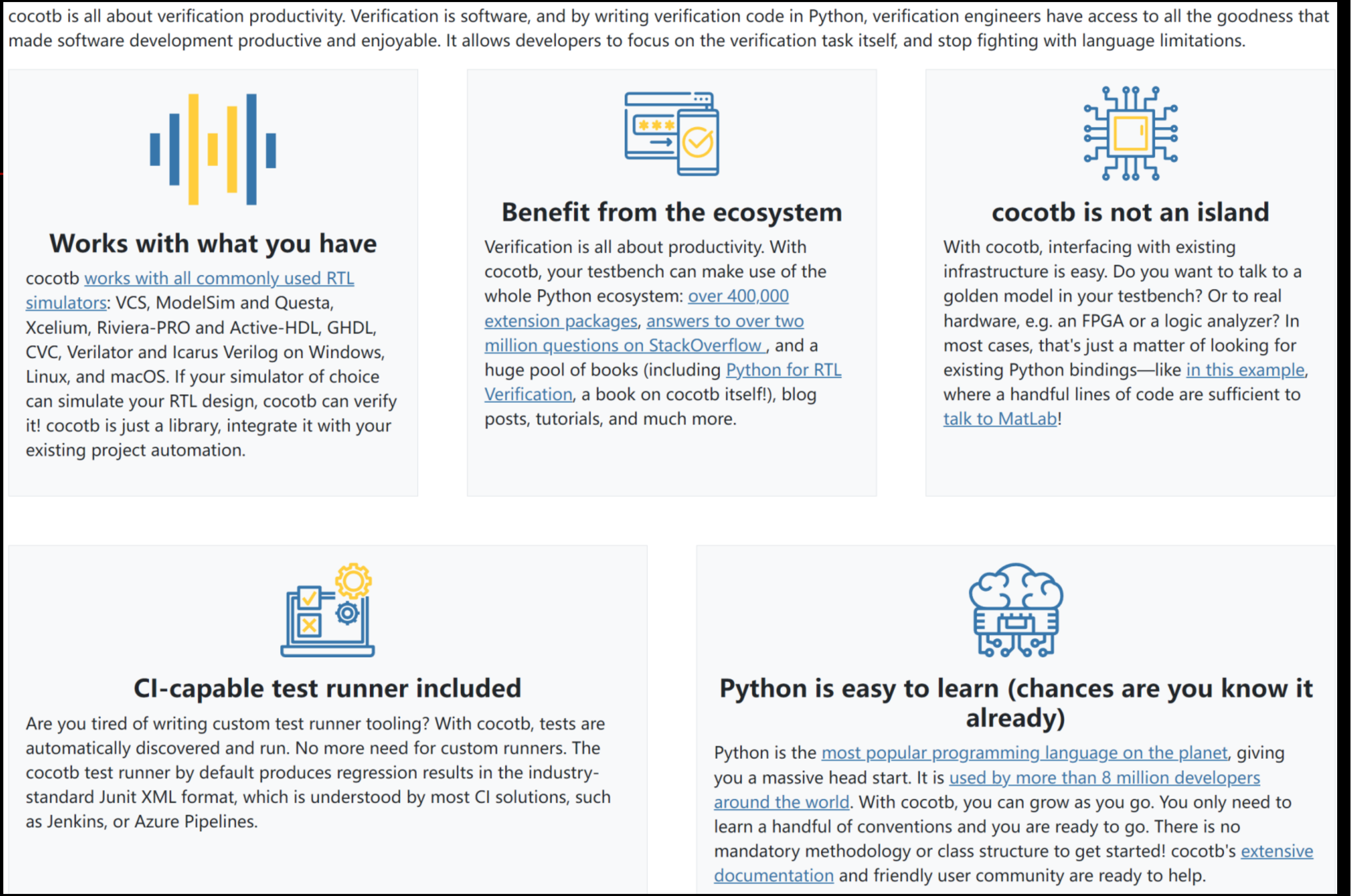
Write a testbench in Python

With cocotb, you write testbenches and verification code in Python. In addition to all the goodies of the Python programming language and its ecosystem, cocotb provides a lean framework to efficiently write verification code .

You are ready to run your test!

Running a test has never been easier thanks to cocotb's built-in test runner with CI integration. Alternatively, you can integrate cocotb easily with your existing build and reporting system.

Key benefits



cocotb is all about verification productivity. Verification is software, and by writing verification code in Python, verification engineers have access to all the goodness that made software development productive and enjoyable. It allows developers to focus on the verification task itself, and stop fighting with language limitations.

Works with what you have

cocotb works with all commonly used RTL simulators: VCS, ModelSim and Questa, Xcelium, Riviera-PRO and Active-HDL, GHDL, CVC, Verilator and Icarus Verilog on Windows, Linux, and macOS. If your simulator of choice can simulate your RTL design, cocotb can verify it! cocotb is just a library, integrate it with your existing project automation.

Benefit from the ecosystem

Verification is all about productivity. With cocotb, your testbench can make use of the whole Python ecosystem: over 400,000 extension packages, answers to over two million questions on StackOverflow , and a huge pool of books (including Python for RTL Verification, a book on cocotb itself!), blog posts, tutorials, and much more.

cocotb is not an island

With cocotb, interfacing with existing infrastructure is easy. Do you want to talk to a golden model in your testbench? Or to real hardware, e.g. an FPGA or a logic analyzer? In most cases, that's just a matter of looking for existing Python bindings—like in this example, where a handful lines of code are sufficient to talk to MatLab!

CI-capable test runner included

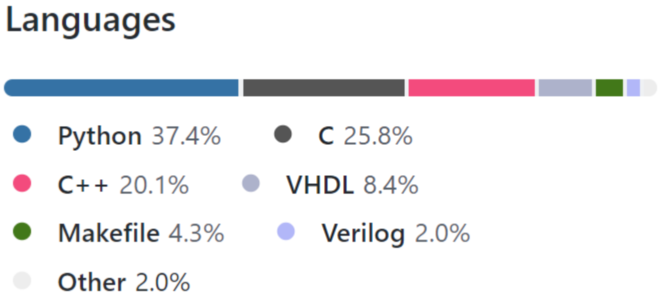
Are you tired of writing custom test runner tooling? With cocotb, tests are automatically discovered and run. No more need for custom runners. The cocotb test runner by default produces regression results in the industry-standard Junit XML format, which is understood by most CI solutions, such as Jenkins, or Azure Pipelines.

Python is easy to learn (chances are you know it already)

Python is the most popular programming language on the planet, giving you a massive head start. It is used by more than 8 million developers around the world. With cocotb, you can grow as you go. You only need to learn a handful of conventions and you are ready to go. There is no mandatory methodology or class structure to get started! cocotb's extensive documentation and friendly user community are ready to help.

Src

- https://github.com/cocotb/cocotb



Languages

● Python 37.4%   ● C 25.8%

● C++ 20.1%   ● VHDL 8.4%

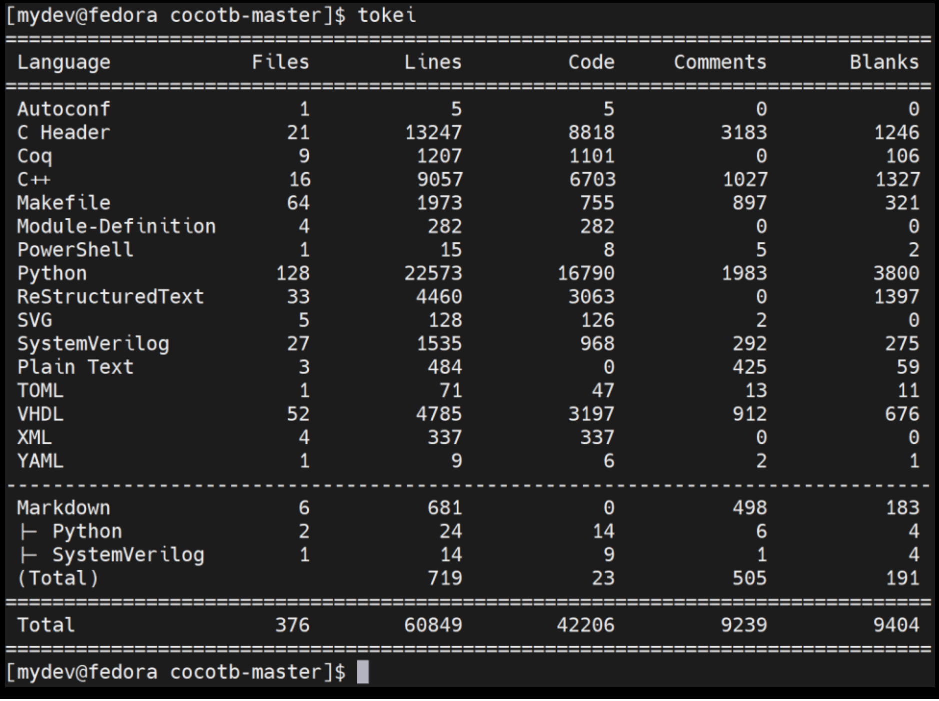
● Makefile 4.3%   ● Verilog 2.0%

● Other 2.0%

Contributors 113

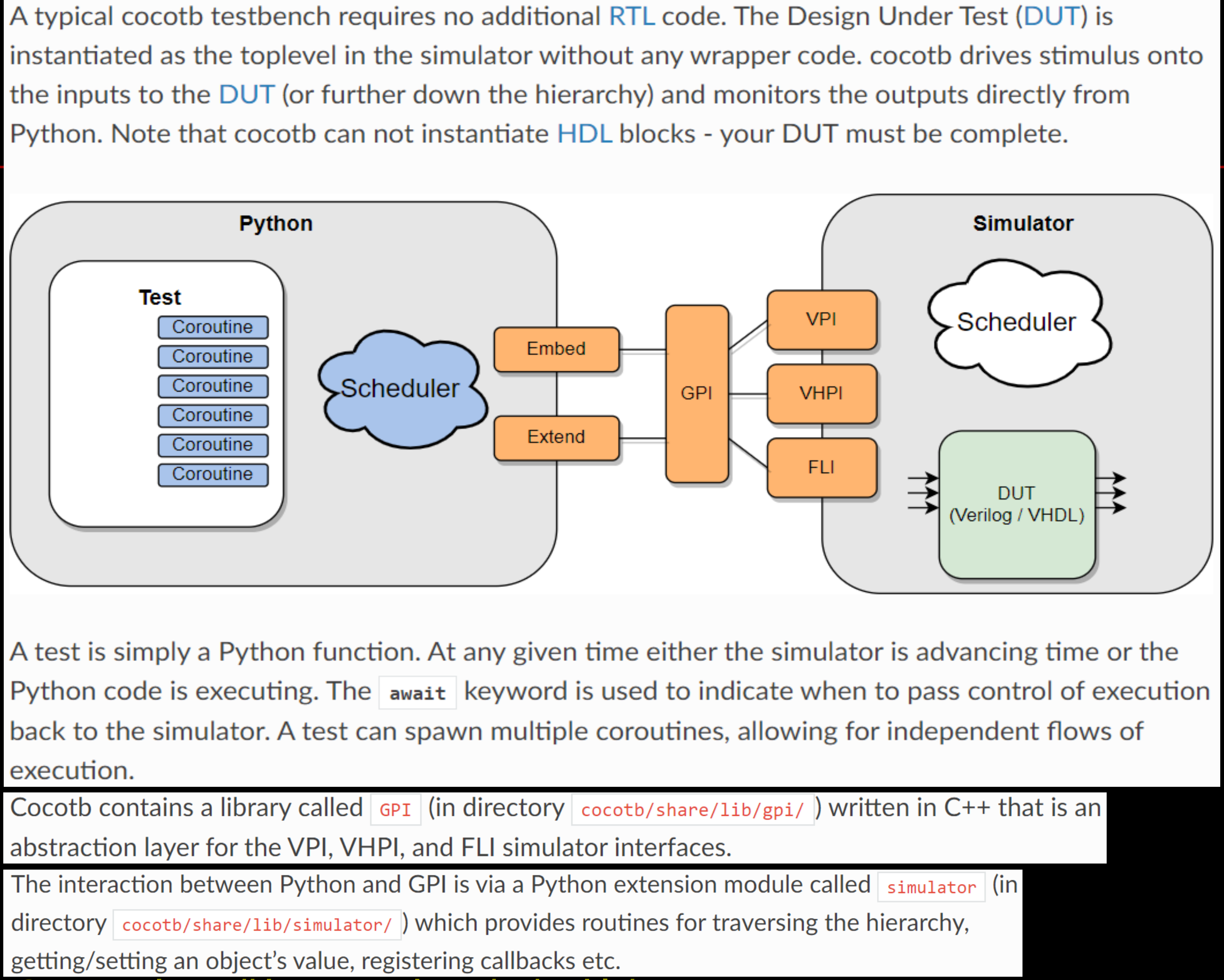
+ 102 contributors

Stats (master branch, last commit: 3602c3d94ca4046ea4ec818e2d3d8bb613de3a7c ~Dec 4, 2022)



```
[mydev@fedora cocotb-master]$ tokei
===============================================================================
 Language            Files        Lines         Code     Comments       Blanks
===============================================================================
 Autoconf                1            5            5            0            0
 C Header               21        13247         8818         3183         1246
 Coq                     9         1207         1101            0          106
 C++                    16         9057         6703         1027         1327
 Makefile               64         1973          755          897          321
 Module-Definition       4          282          282            0            0
 PowerShell              1           15            8            5            2
 Python                128        22573        16790         1983         3800
 ReStructuredText       33         4460         3063            0         1397
 SVG                     5          128          126            2            0
 SystemVerilog          27         1535          968          292          275
 Plain Text              3          484            0          425           59
 TOML                    1           71           47           13           11
 VHDL                   52         4785         3197          912          676
 XML                     4          337          337            0            0
 YAML                    1            9            6            2            1
-------------------------------------------------------------------------------
 Markdown                6          681            0          498          183
 |- Python               2           24           14            6            4
 |- SystemVerilog        1           14            9            1            4
 (Total)                            719           23          505          191
===============================================================================
 Total                 376        60849        42206         9239         9404
===============================================================================
[mydev@fedora cocotb-master]$ █
```

Workflow



A typical cocotb testbench requires no additional RTL code. The Design Under Test (DUT) is instantiated as the toplevel in the simulator without any wrapper code. cocotb drives stimulus onto the inputs to the DUT (or further down the hierarchy) and monitors the outputs directly from Python. Note that cocotb can not instantiate HDL blocks - your DUT must be complete.

A test is simply a Python function. At any given time either the simulator is advancing time or the Python code is executing. The `await` keyword is used to indicate when to pass control of execution back to the simulator. A test can spawn multiple coroutines, allowing for independent flows of execution.

Cocotb contains a library called `GPI` (in directory `cocotb/share/lib/gpi/`) written in C++ that is an abstraction layer for the VPI, VHPI, and FLI simulator interfaces.

The interaction between Python and GPI is via a Python extension module called `simulator` (in directory `cocotb/share/lib/simulator/`) which provides routines for traversing the hierarchy, getting/setting an object's value, registering callbacks etc.

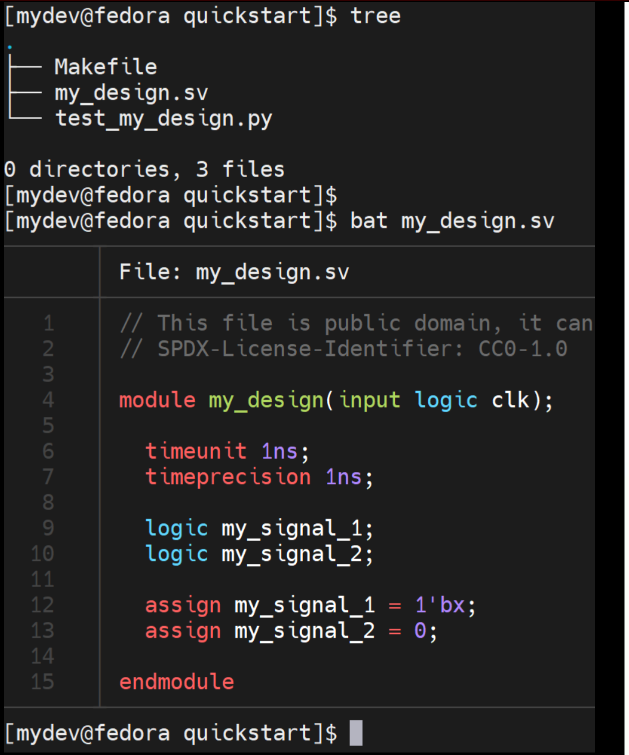
Source: https://docs.cocotb.org/en/stable/

- https://docs.python.org/3/glossary.html#term-coroutine

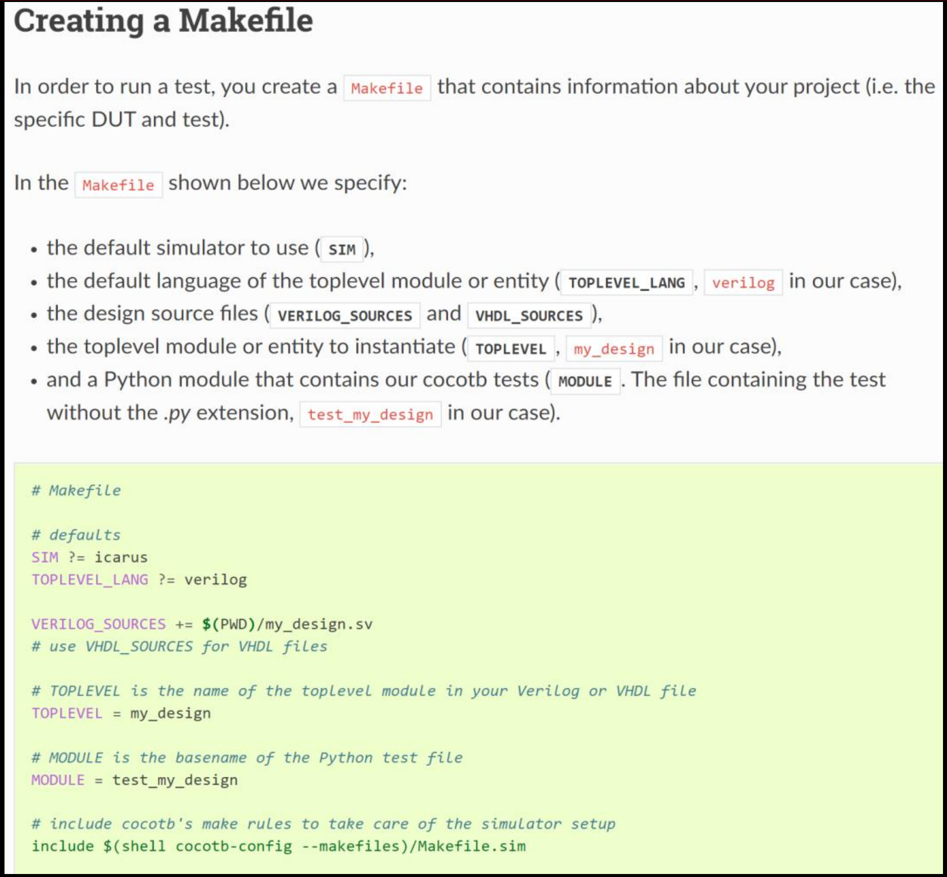
2.3.2 Examples

Quickstart

- https://docs.cocotb.org/en/stable/quickstart.html
  $SRC_COCOTB/examples/doc_examples/quickstart



```
[mydev@fedora quickstart]$ tree
.
├── Makefile
├── my_design.sv
└── test_my_design.py

0 directories, 3 files
[mydev@fedora quickstart]$
[mydev@fedora quickstart]$ bat my_design.sv
───────┬────────────────────────────────────
       │ File: my_design.sv
───────┼────────────────────────────────────
       │ // This file is public domain, it can
       │ // SPDX-License-Identifier: CC0-1.0
       │
       │ module my_design(input logic clk);
       │
       │   timeunit 1ns;
       │   timeprecision 1ns;
       │
       │   logic my_signal_1;
       │   logic my_signal_2;
       │
       │   assign my_signal_1 = 1'bx;
       │   assign my_signal_2 = 0;
       │
       │ endmodule
───────┴────────────────────────────────────
[mydev@fedora quickstart]$
```



Creating a Makefile

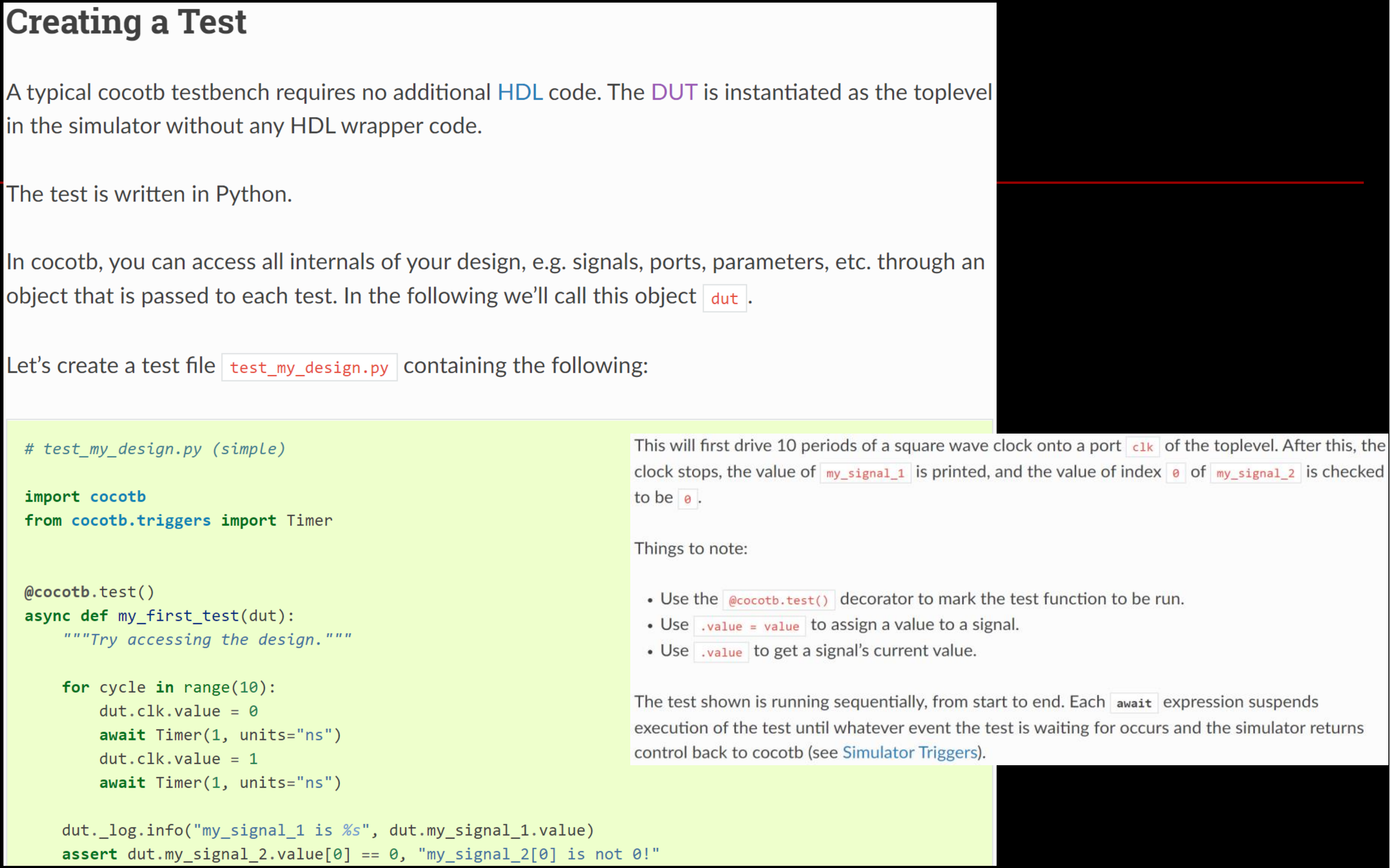
In order to run a test, you create a `Makefile` that contains information about your project (i.e. the specific DUT and test).

In the `Makefile` shown below we specify:

- the default simulator to use (`SIM`),
- the default language of the toplevel module or entity (`TOPLEVEL_LANG` , `verilog` in our case),
- the design source files (`VERILOG_SOURCES` and `VHDL_SOURCES`),
- the toplevel module or entity to instantiate (`TOPLEVEL` , `my_design` in our case),
- and a Python module that contains our cocotb tests (`MODULE` . The file containing the test without the *.py* extension, `test_my_design` in our case).

```
# Makefile

# defaults
SIM ?= icarus
TOPLEVEL_LANG ?= verilog

VERILOG_SOURCES += $(PWD)/my_design.sv
# use VHDL_SOURCES for VHDL files

# TOPLEVEL is the name of the toplevel module in your Verilog or VHDL file
TOPLEVEL = my_design

# MODULE is the basename of the Python test file
MODULE = test_my_design

# include cocotb's make rules to take care of the simulator setup
include $(shell cocotb-config --makefiles)/Makefile.sim
```

Cocotb testbench:



Creating a Test

A typical cocotb testbench requires no additional HDL code. The DUT is instantiated as the toplevel in the simulator without any HDL wrapper code.

The test is written in Python.

In cocotb, you can access all internals of your design, e.g. signals, ports, parameters, etc. through an object that is passed to each test. In the following we'll call this object `dut`.

Let's create a test file `test_my_design.py` containing the following:

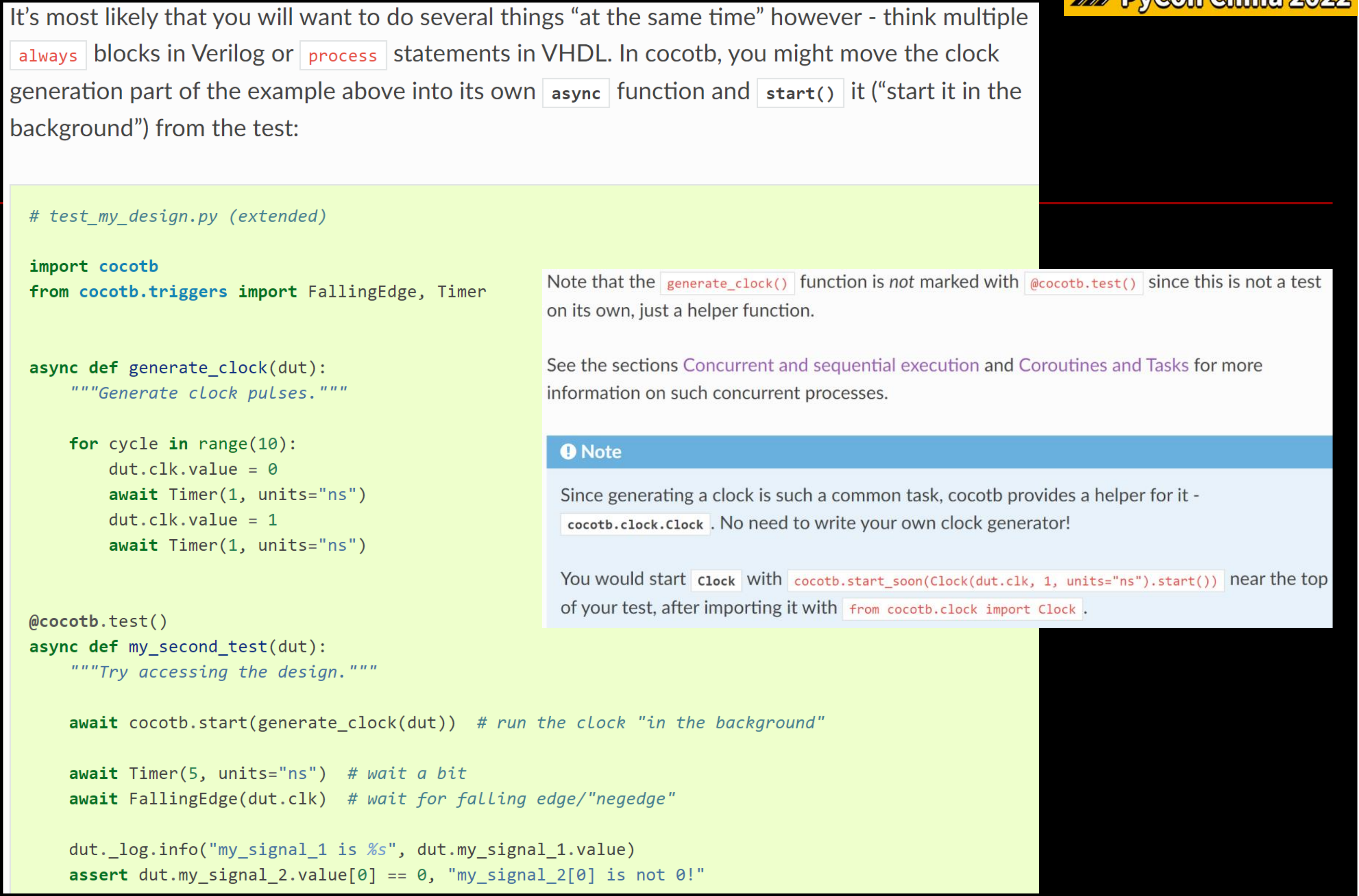
```python
# test_my_design.py (simple)

import cocotb
from cocotb.triggers import Timer


@cocotb.test()
async def my_first_test(dut):
    """Try accessing the design."""

    for cycle in range(10):
        dut.clk.value = 0
        await Timer(1, units="ns")
        dut.clk.value = 1
        await Timer(1, units="ns")

    dut._log.info("my_signal_1 is %s", dut.my_signal_1.value)
    assert dut.my_signal_2.value[0] == 0, "my_signal_2[0] is not 0!"
```

This will first drive 10 periods of a square wave clock onto a port `clk` of the toplevel. After this, the clock stops, the value of `my_signal_1` is printed, and the value of index `0` of `my_signal_2` is checked to be `0`.

Things to note:

- Use the `@cocotb.test()` decorator to mark the test function to be run.
- Use `.value = value` to assign a value to a signal.
- Use `.value` to get a signal's current value.

The test shown is running sequentially, from start to end. Each `await` expression suspends execution of the test until whatever event the test is waiting for occurs and the simulator returns control back to cocotb (see Simulator Triggers).



It’s most likely that you will want to do several things “at the same time” however - think multiple `always` blocks in Verilog or `process` statements in VHDL. In cocotb, you might move the clock generation part of the example above into its own `async` function and `start()` it (“start it in the background”) from the test:

```
# test_my_design.py (extended)

import cocotb
from cocotb.triggers import FallingEdge, Timer


async def generate_clock(dut):
    """Generate clock pulses."""

    for cycle in range(10):
        dut.clk.value = 0
        await Timer(1, units="ns")
        dut.clk.value = 1
        await Timer(1, units="ns")


@cocotb.test()
async def my_second_test(dut):
    """Try accessing the design."""

    await cocotb.start(generate_clock(dut))  # run the clock "in the background"

    await Timer(5, units="ns")  # wait a bit
    await FallingEdge(dut.clk)  # wait for falling edge/"negedge"

    dut._log.info("my_signal_1 is %s", dut.my_signal_1.value)
    assert dut.my_signal_2.value[0] == 0, "my_signal_2[0] is not 0!"
```

Note that the `generate_clock()` function is *not* marked with `@cocotb.test()` since this is not a test on its own, just a helper function.

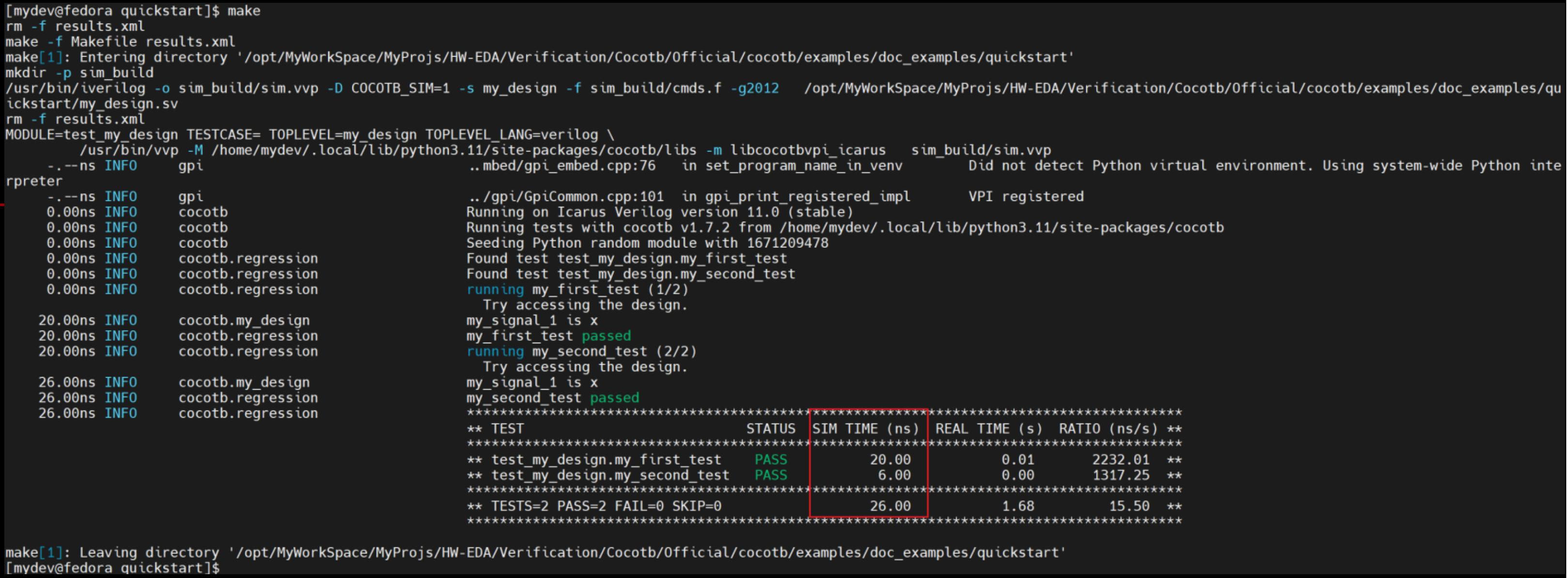
See the sections Concurrent and sequential execution and Coroutines and Tasks for more information on such concurrent processes.

Note

Since generating a clock is such a common task, cocotb provides a helper for it - `cocotb.clock.Clock`. No need to write your own clock generator!

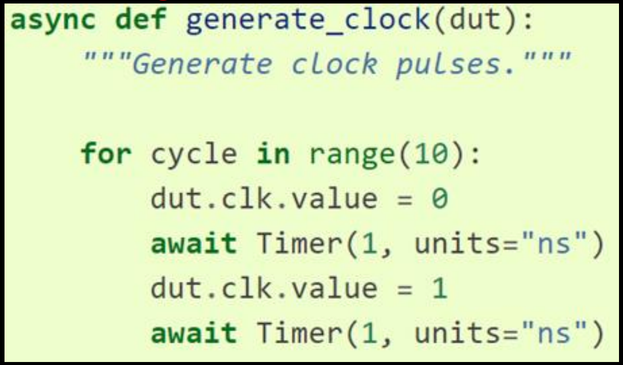
You would start `Clock` with `cocotb.start_soon(Clock(dut.clk, 1, units="ns").start())` near the top of your test, after importing it with `from cocotb.clock import Clock`.

run the testbench:

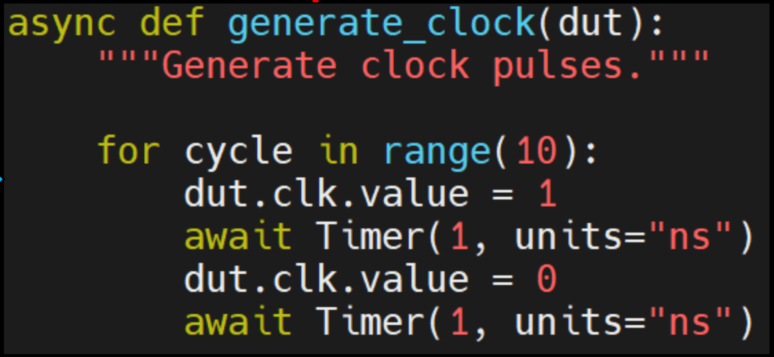


```
[mydev@fedora quickstart]$ make
rm -f results.xml
make -f Makefile results.xml
make[1]: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/cocotb/examples/doc_examples/quickstart'
mkdir -p sim_build
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s my_design -f sim_build/cmds.f -g2012   /opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/cocotb/examples/doc_examples/qu
ickstart/my_design.sv
rm -f results.xml
MODULE=test_my_design TESTCASE= TOPLEVEL=my_design TOPLEVEL_LANG=verilog \
         /usr/bin/vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:76   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python inte
rpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.7.2 from /home/mydev/.local/lib/python3.11/site-packages/cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1671209478
     0.00ns INFO     cocotb.regression                  Found test test_my_design.my_first_test
     0.00ns INFO     cocotb.regression                  Found test test_my_design.my_second_test
     0.00ns INFO     cocotb.regression                  running my_first_test (1/2)
                                                          Try accessing the design.
    20.00ns INFO     cocotb.my_design                   my_signal_1 is x
    20.00ns INFO     cocotb.regression                  my_first_test passed
    20.00ns INFO     cocotb.regression                  running my_second_test (2/2)
                                                          Try accessing the design.
    26.00ns INFO     cocotb.my_design                   my_signal_1 is x
    26.00ns INFO     cocotb.regression                  my_second_test passed
    26.00ns INFO     cocotb.regression                  *****************************************************************************************
                                                        ** TEST                             STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                        *****************************************************************************************
                                                        ** test_my_design.my_first_test      PASS          20.00           0.01       2232.01  **
                                                        ** test_my_design.my_second_test     PASS           6.00           0.00       1317.25  **
                                                        *****************************************************************************************
                                                        ** TESTS=2 PASS=2 FAIL=0 SKIP=0                    26.00           1.68         15.50  **
                                                        *****************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/cocotb/examples/doc_examples/quickstart'
[mydev@fedora quickstart]$
```

exchange the order for value assignment of the square wave clock:

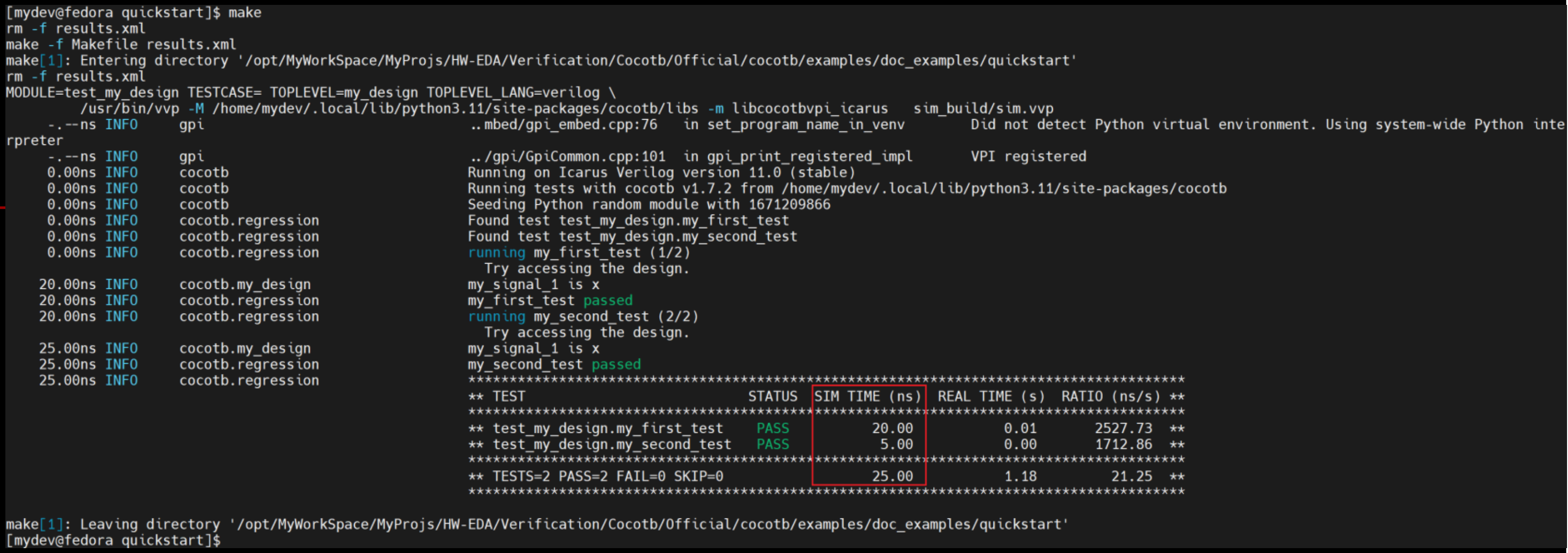


```python
async def generate_clock(dut):
    """Generate clock pulses."""

    for cycle in range(10):
        dut.clk.value = 0
        await Timer(1, units="ns")
        dut.clk.value = 1
        await Timer(1, units="ns")
```



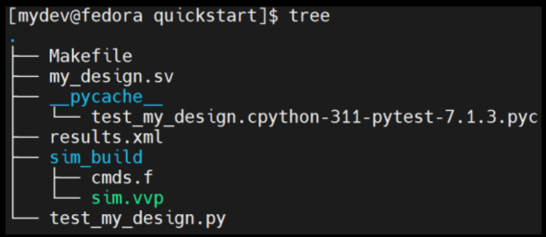
```python
async def generate_clock(dut):
    """Generate clock pulses."""

    for cycle in range(10):
        dut.clk.value = 1
        await Timer(1, units="ns")
        dut.clk.value = 0
        await Timer(1, units="ns")
```

rerun the testbench:

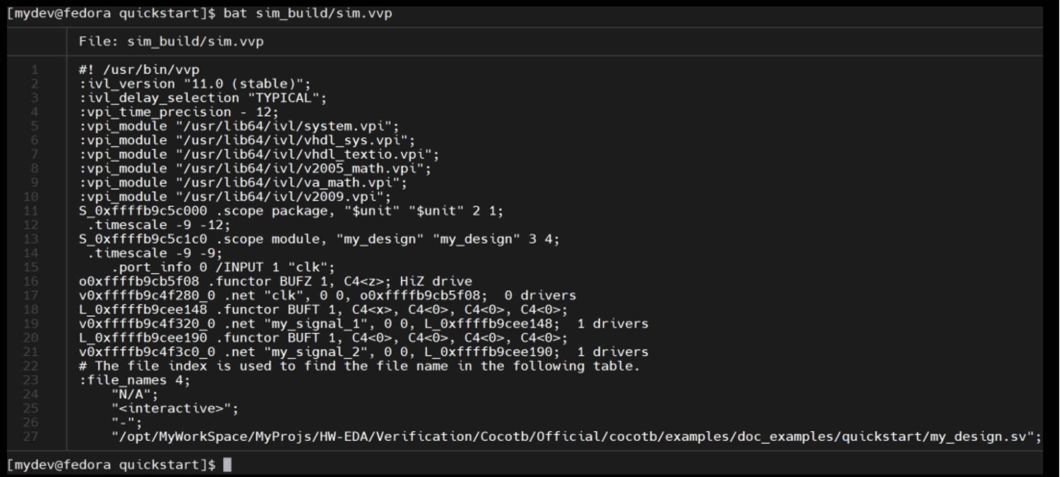


```
[mydev@fedora quickstart]$ make
rm -f results.xml
make -f Makefile results.xml
make[1]: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/cocotb/examples/doc_examples/quickstart'
rm -f results.xml
MODULE=test_my_design TESTCASE= TOPLEVEL=my_design TOPLEVEL_LANG=verilog \
         /usr/bin/vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:76   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python inte
rpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                            Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                            Running tests with cocotb v1.7.2 from /home/mydev/.local/lib/python3.11/site-packages/cocotb
     0.00ns INFO     cocotb                            Seeding Python random module with 1671209866
     0.00ns INFO     cocotb.regression                 Found test test_my_design.my_first_test
     0.00ns INFO     cocotb.regression                 Found test test_my_design.my_second_test
     0.00ns INFO     cocotb.regression                 running my_first_test (1/2)
                                                         Try accessing the design.
    20.00ns INFO     cocotb.my_design                  my_signal_1 is x
    20.00ns INFO     cocotb.regression                 my_first_test passed
    20.00ns INFO     cocotb.regression                 running my_second_test (2/2)
                                                         Try accessing the design.
    25.00ns INFO     cocotb.my_design                  my_signal_1 is x
    25.00ns INFO     cocotb.regression                 my_second_test passed
    25.00ns INFO     cocotb.regression                 **************************************************************************************
                                                       ** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                       **************************************************************************************
                                                       ** test_my_design.my_first_test   PASS          20.00           0.01       2527.73  **
                                                       ** test_my_design.my_second_test  PASS           5.00           0.00       1712.86  **
                                                       **************************************************************************************
                                                       ** TESTS=2 PASS=2 FAIL=0 SKIP=0                 25.00           1.18         21.25  **
                                                       **************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/cocotb/examples/doc_examples/quickstart'
[mydev@fedora quickstart]$
```

...



```
[mydev@fedora quickstart]$ tree
.
├── Makefile
├── my_design.sv
├── __pycache__
│   └── test_my_design.cpython-311-pytest-7.1.3.pyc
├── results.xml
├── sim_build
│   ├── cmds.f
│   └── sim.vvp
└── test_my_design.py
```



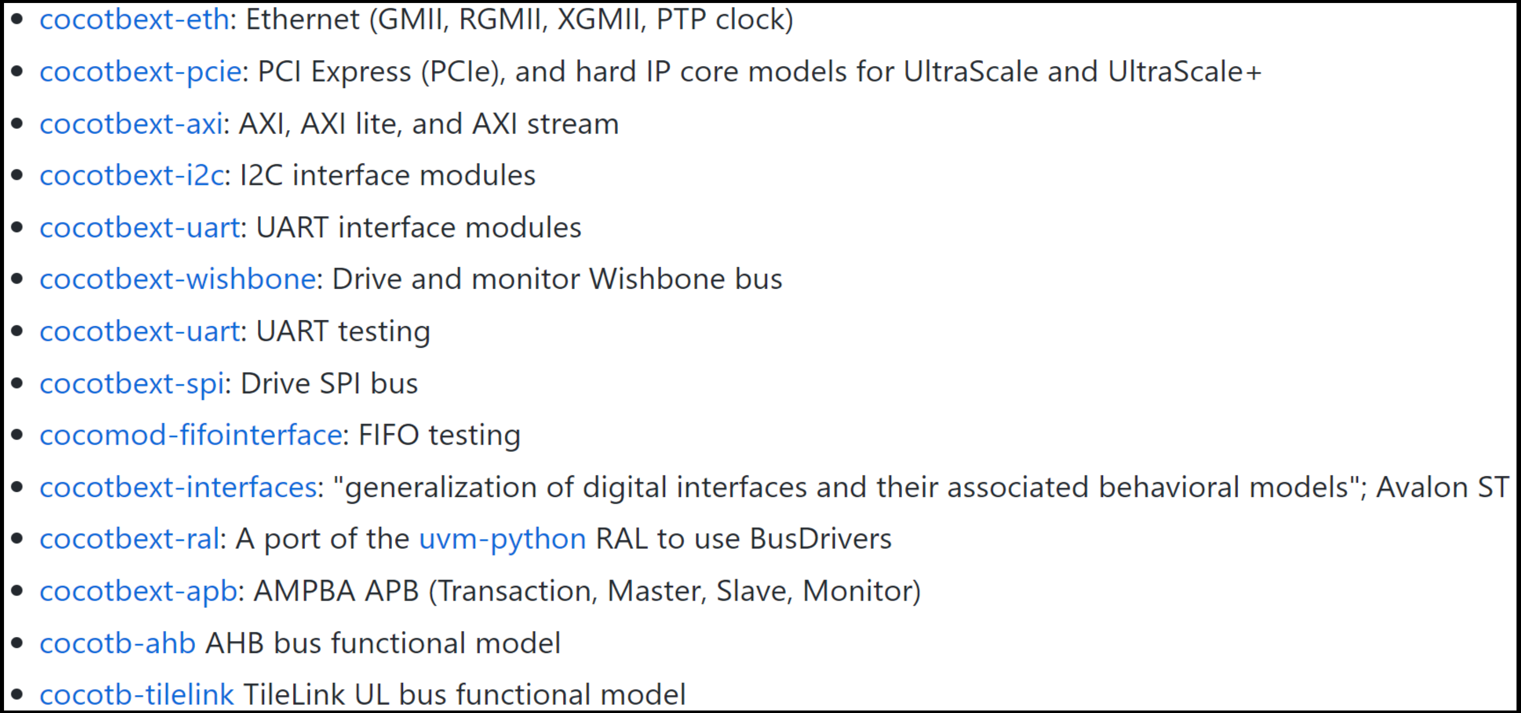
```
[mydev@fedora quickstart]$ bat sim_build/sim.vvp
       File: sim_build/sim.vvp
       #! /usr/bin/vvp
       :ivl_version "11.0 (stable)";
       :ivl_delay_selection "TYPICAL";
       :vpi_time_precision - 12;
       :vpi_module "/usr/lib64/ivl/system.vpi";
       :vpi_module "/usr/lib64/ivl/vhdl_sys.vpi";
       :vpi_module "/usr/lib64/ivl/vhdl_textio.vpi";
       :vpi_module "/usr/lib64/ivl/v2005_math.vpi";
       :vpi_module "/usr/lib64/ivl/va_math.vpi";
       :vpi_module "/usr/lib64/ivl/v2009.vpi";
       S_0xffffb9c5c000 .scope package, "$unit" "$unit" 2 1;
        .timescale -9 -12;
       S_0xffffb9c5c1c0 .scope module, "my_design" "my_design" 3 4;
        .timescale -9 -9;
           .port_info 0 /INPUT 1 "clk";
       o0xffffb9cb5f08 .functor BUFZ 1, C4<z>; HiZ drive
       v0xffffb9c4f280_0 .net "clk", 0 0, o0xffffb9cb5f08;  0 drivers
       L_0xffffb9cee148 .functor BUFT 1, C4<x>, C4<0>, C4<0>, C4<0>;
       v0xffffb9c4f320_0 .net "my_signal_1", 0 0, L_0xffffb9cee148;  1 drivers
       L_0xffffb9cee190 .functor BUFT 1, C4<0>, C4<0>, C4<0>, C4<0>;
       v0xffffb9c4f3c0_0 .net "my_signal_2", 0 0, L_0xffffb9cee190;  1 drivers
       # The file index is used to find the file name in the following table.
       :file_names 4;
           "N/A";
           "<interactive>";
           "-";
           "/opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/cocotb/examples/doc_examples/quickstart/my_design.sv";
[mydev@fedora quickstart]$ █
```

2.3.3 Extensions

Good Resources

- https://docs.cocotb.org/en/stable/extensions.html
- https://github.com/cocotb/cocotb/wiki/Further-Resources

…



- cocotbext-eth: Ethernet (GMII, RGMII, XGMII, PTP clock)
- cocotbext-pcie: PCI Express (PCIe), and hard IP core models for UltraScale and UltraScale+
- cocotbext-axi: AXI, AXI lite, and AXI stream
- cocotbext-i2c: I2C interface modules
- cocotbext-uart: UART interface modules
- cocotbext-wishbone: Drive and monitor Wishbone bus
- cocotbext-uart: UART testing
- cocotbext-spi: Drive SPI bus
- cocomod-fifointerface: FIFO testing
- cocotbext-interfaces: "generalization of digital interfaces and their associated behavioral models"; Avalon ST
- cocotbext-ral: A port of the uvm-python RAL to use BusDrivers
- cocotbext-apb: AMPBA APB (Transaction, Master, Slave, Monitor)
- cocotb-ahb AHB bus functional model
- cocotb-tilelink TileLink UL bus functional model

…

- https://github.com/cocotb/cocotb/blob/master/documentation/source/extensions.rst
- …

2.3.4 Cocotb vs UVM

Good Resources

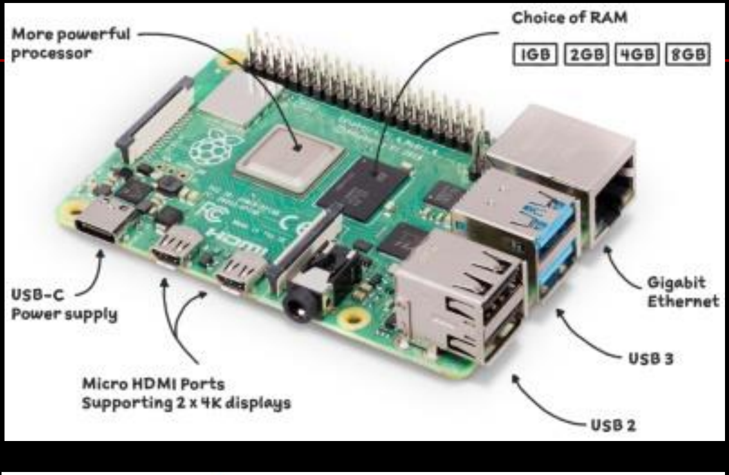
- https://www.reddit.com/r/FPGA/comments/v8fd63/cocotb_in_python_vs_uvm_in_systemverilog/
- …

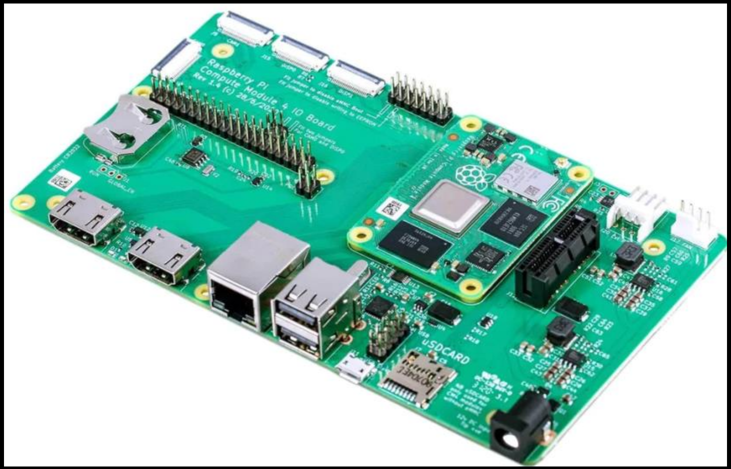
Python for Good
PyCon China 2022

3) Testbed

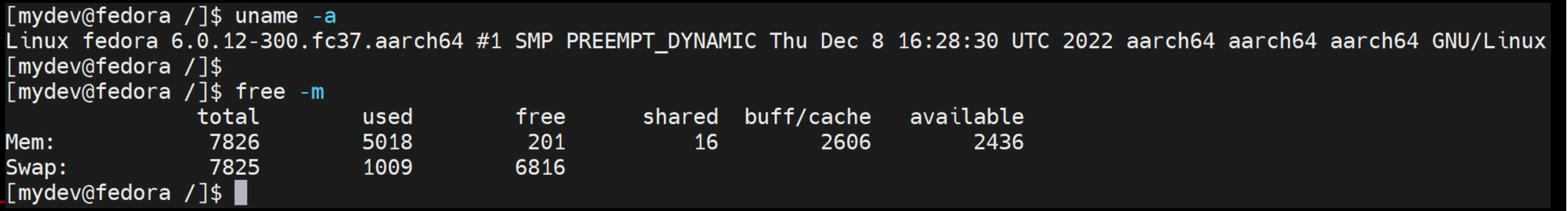
3.1 Raspberry Pi 4(8GB LPDDR4) with Fedora 37

- HW env

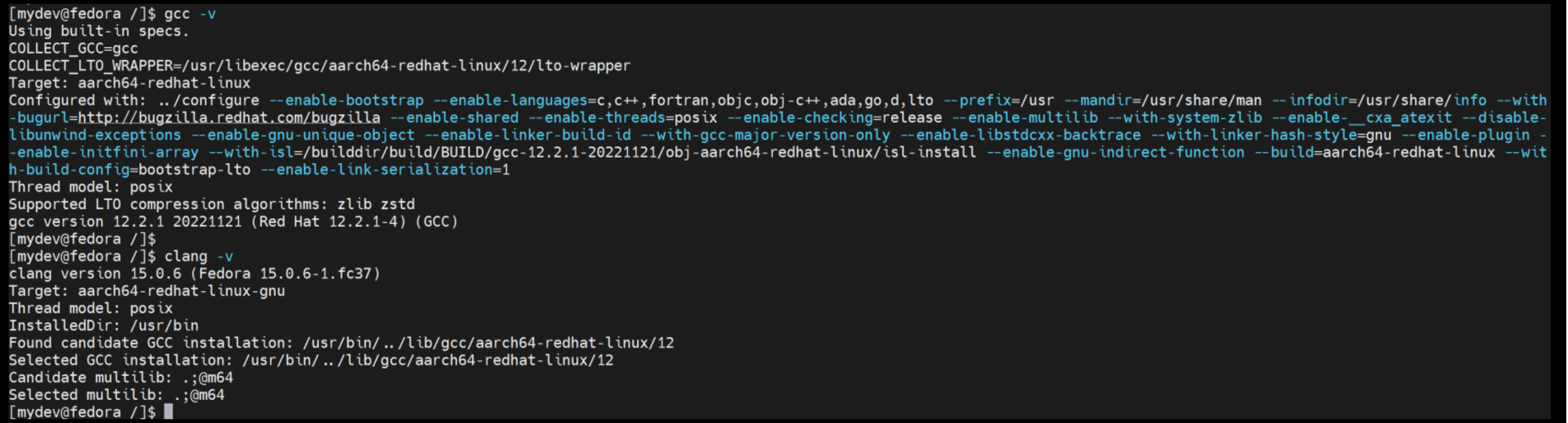




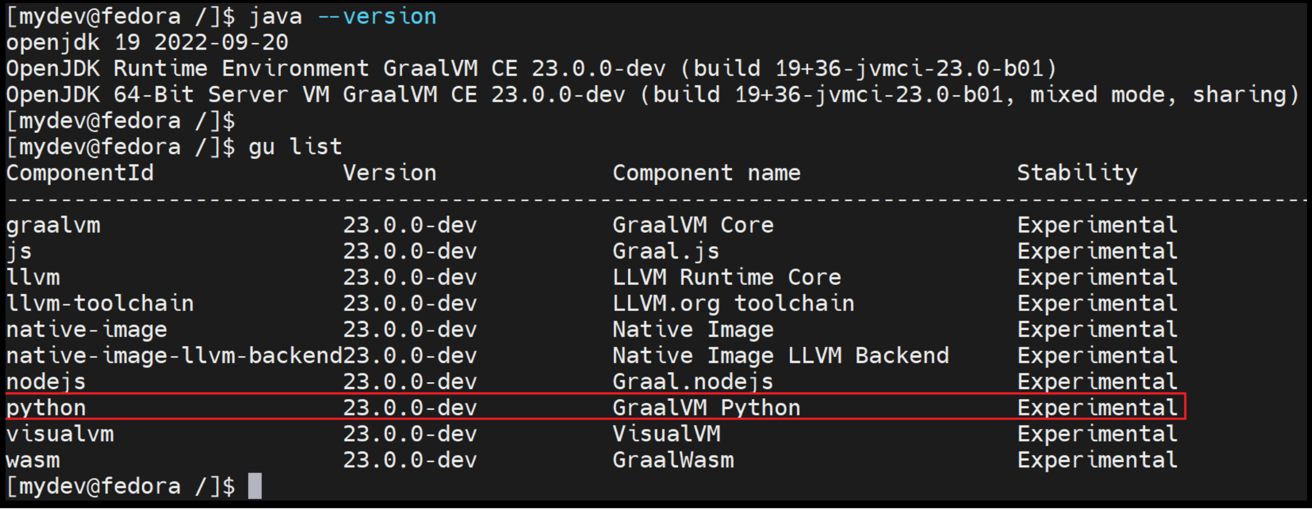
SW env



```
[mydev@fedora /]$ uname -a
Linux fedora 6.0.12-300.fc37.aarch64 #1 SMP PREEMPT_DYNAMIC Thu Dec 8 16:28:30 UTC 2022 aarch64 aarch64 aarch64 GNU/Linux
[mydev@fedora /]$
[mydev@fedora /]$ free -m
               total        used        free      shared  buff/cache   available
Mem:            7826        5018         201          16        2606        2436
Swap:           7825        1009        6816
[mydev@fedora /]$
```



```
[mydev@fedora /]$ gcc -v
Using built-in specs.
COLLECT_GCC=gcc
COLLECT_LTO_WRAPPER=/usr/libexec/gcc/aarch64-redhat-linux/12/lto-wrapper
Target: aarch64-redhat-linux
Configured with: ../configure --enable-bootstrap --enable-languages=c,c++,fortran,objc,obj-c++,ada,go,d,lto --prefix=/usr --mandir=/usr/share/man --infodir=/usr/share/info --with
-bugurl=http://bugzilla.redhat.com/bugzilla --enable-shared --enable-threads=posix --enable-checking=release --enable-multilib --with-system-zlib --enable-__cxa_atexit --disable-
libunwind-exceptions --enable-gnu-unique-object --enable-linker-build-id --with-gcc-major-version-only --enable-libstdcxx-backtrace --with-linker-hash-style=gnu --enable-plugin -
-enable-initfini-array --with-isl=/builddir/build/BUILD/gcc-12.2.1-20221121/obj-aarch64-redhat-linux/isl-install --enable-gnu-indirect-function --build=aarch64-redhat-linux --wit
h-build-config=bootstrap-lto --enable-link-serialization=1
Thread model: posix
Supported LTO compression algorithms: zlib zstd
gcc version 12.2.1 20221121 (Red Hat 12.2.1-4) (GCC)
[mydev@fedora /]$
[mydev@fedora /]$ clang -v
clang version 15.0.6 (Fedora 15.0.6-1.fc37)
Target: aarch64-redhat-linux-gnu
Thread model: posix
InstalledDir: /usr/bin
Found candidate GCC installation: /usr/bin/../lib/gcc/aarch64-redhat-linux/12
Selected GCC installation: /usr/bin/../lib/gcc/aarch64-redhat-linux/12
Candidate multilib: .;@m64
Selected multilib: .;@m64
[mydev@fedora /]$
```



```
[mydev@fedora /]$ java --version
openjdk 19 2022-09-20
OpenJDK Runtime Environment GraalVM CE 23.0.0-dev (build 19+36-jvmci-23.0-b01)
OpenJDK 64-Bit Server VM GraalVM CE 23.0.0-dev (build 19+36-jvmci-23.0-b01, mixed mode, sharing)
[mydev@fedora /]$
[mydev@fedora /]$ gu list
ComponentId              Version             Component name                Stability
-----------------------------------------------------------------------------------------------
graalvm                  23.0.0-dev          GraalVM Core                  Experimental
js                       23.0.0-dev          Graal.js                      Experimental
llvm                     23.0.0-dev          LLVM Runtime Core             Experimental
llvm-toolchain           23.0.0-dev          LLVM.org toolchain            Experimental
native-image             23.0.0-dev          Native Image                  Experimental
native-image-llvm-backend23.0.0-dev          Native Image LLVM Backend     Experimental
nodejs                   23.0.0-dev          Graal.nodejs                  Experimental
python                   23.0.0-dev          GraalVM Python                Experimental
visualvm                 23.0.0-dev          VisualVM                      Experimental
wasm                     23.0.0-dev          GraalWasm                     Experimental
[mydev@fedora /]$
```

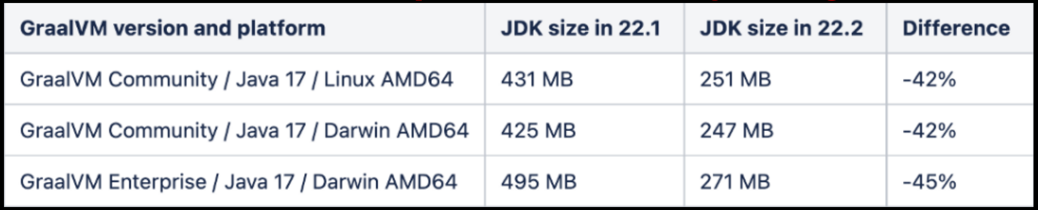
By the way: current release and roadmap of GraalVM

- https://medium.com/graalvm/announcing-the-graalvm-community-roadmap-b8d77201b497

GraalVM 22.2

- https://medium.com/graalvm/graalvm-22-2-smaller-jdk-size-improved-memory-usage-better-library-support-and-more-cb34b5b68ec0

Smaller JDK size, improved memory usage, better library support, and more!



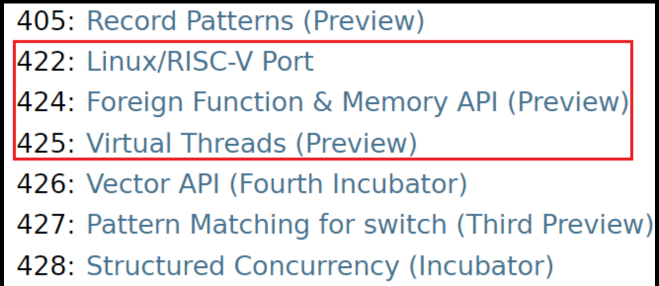
GraalVM version and platform	JDK size in 22.1	JDK size in 22.2	Difference
GraalVM Community / Java 17 / Linux AMD64	431 MB	251 MB	-42%
GraalVM Community / Java 17 / Darwin AMD64	425 MB	247 MB	-42%
GraalVM Enterprise / Java 17 / Darwin AMD64	495 MB	271 MB	-45%

…

JDK 19

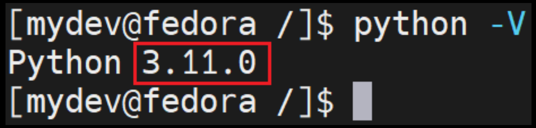
- https://openjdk.java.net/projects/jdk/19/

Features

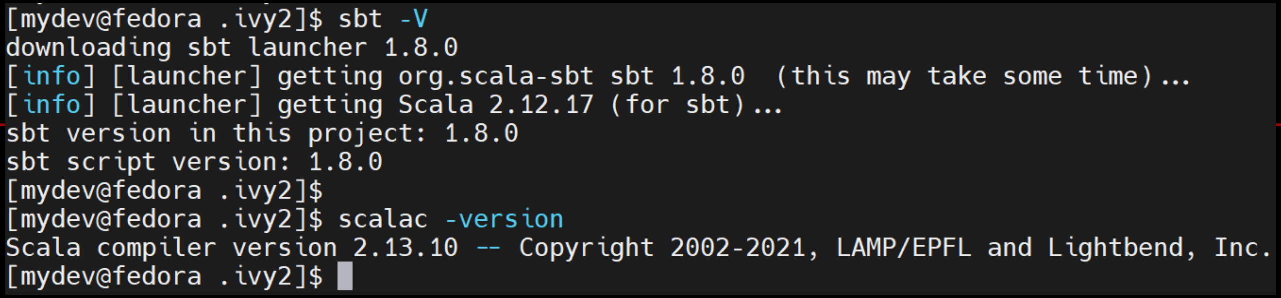


405: Record Patterns (Preview)
422: Linux/RISC-V Port
424: Foreign Function & Memory API (Preview)
425: Virtual Threads (Preview)
426: Vector API (Fourth Incubator)
427: Pattern Matching for switch (Third Preview)
428: Structured Concurrency (Incubator)

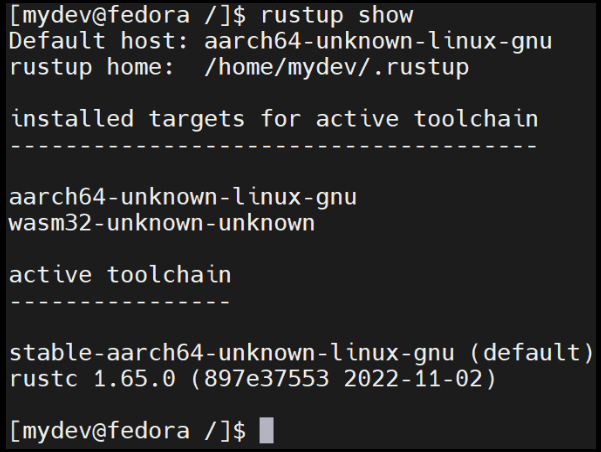
- https://jdk.java.net/19/release-notes



```
[mydev@fedora /]$ python -V
Python 3.11.0
[mydev@fedora /]$ 
```



```
[mydev@fedora .ivy2]$ sbt -V
downloading sbt launcher 1.8.0
[info] [launcher] getting org.scala-sbt sbt 1.8.0  (this may take some time)...
[info] [launcher] getting Scala 2.12.17 (for sbt)...
sbt version in this project: 1.8.0
sbt script version: 1.8.0
[mydev@fedora .ivy2]$
[mydev@fedora .ivy2]$ scalac -version
Scala compiler version 2.13.10 -- Copyright 2002-2021, LAMP/EPFL and Lightbend, Inc.
[mydev@fedora .ivy2]$ 
```



```
[mydev@fedora /]$ rustup show
Default host: aarch64-unknown-linux-gnu
rustup home:  /home/mydev/.rustup

installed targets for active toolchain
--------------------------------------

aarch64-unknown-linux-gnu
wasm32-unknown-unknown

active toolchain
----------------

stable-aarch64-unknown-linux-gnu (default)
rustc 1.65.0 (897e37553 2022-11-02)

[mydev@fedora /]$ 
```

3.1.1 Fedora

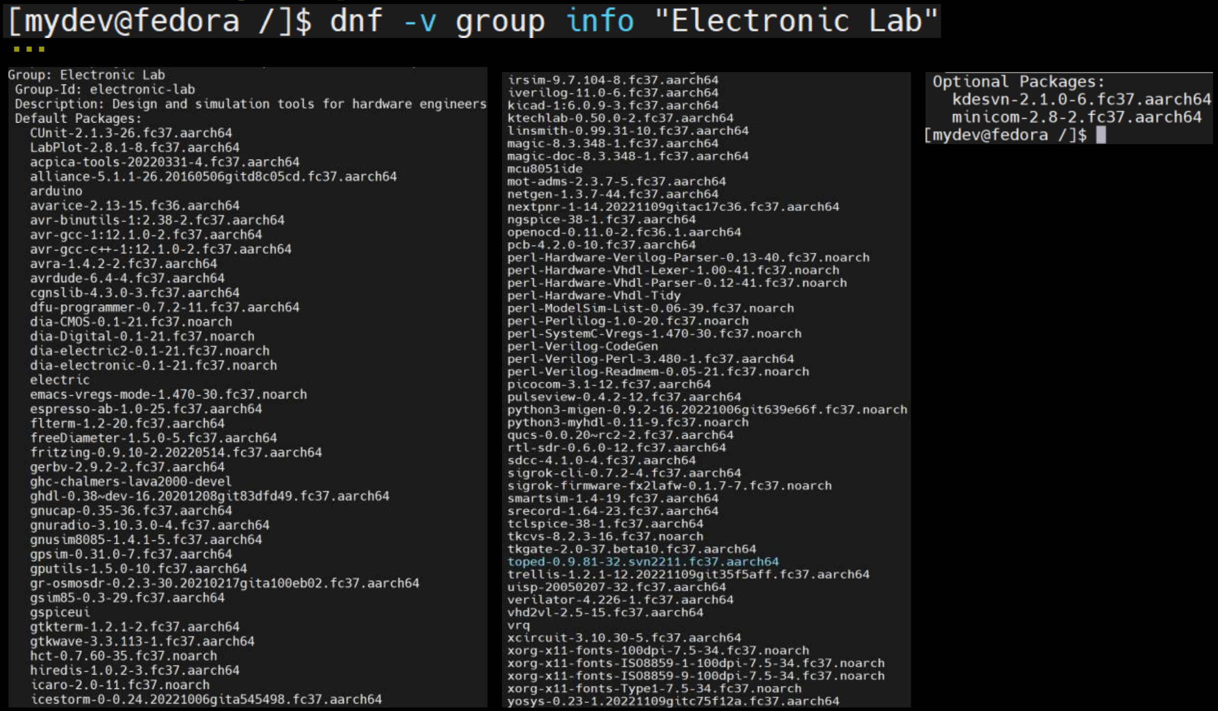
- A Linux distribution developed by the community-supported Fedora Project which is sponsored primarily by Red Hat.
- https://en.wikipedia.org/wiki/Fedora_(operating_system)
- https://getfedora.org/
- https://alt.fedoraproject.org/alt/
- https://spins.fedoraproject.org/
- https://fedoraproject.org/wiki/Architectures/ARM
- https://fedoramagazine.org/
- https://silverblue.fedoraproject.org/
- https://fedoraproject.org/wiki/Changes/RaspberryPi4
- Developer friendly!

3.1.1.1 EDA support

- https://fedoraproject.org/wiki/Electronic_Lab

Installation

- sudo dnf groupinstall "Electronic Lab"



```
[mydev@fedora /]$ dnf -v group info "Electronic Lab"
...
```

```
Group: Electronic Lab
 Group-Id: electronic-lab
 Description: Design and simulation tools for hardware engineers
 Default Packages:
   CUnit-2.1.3-26.fc37.aarch64
   LabPlot-2.8.1-8.fc37.aarch64
   acpica-tools-20220331-4.fc37.aarch64
   alliance-5.1.1-26.20160506gitd8c05cd.fc37.aarch64
   arduino
   avarice-2.13-15.fc36.aarch64
   avr-binutils-1:2.38-2.fc37.aarch64
   avr-gcc-1:12.1.0-2.fc37.aarch64
   avr-gcc-c++-1:12.1.0-2.fc37.aarch64
   avra-1.4.2-2.fc37.aarch64
   avrdude-6.4-4.fc37.aarch64
   cgnslib-4.3.0-3.fc37.aarch64
   dfu-programmer-0.7.2-11.fc37.aarch64
   dia-CMOS-0.1-21.fc37.noarch
   dia-Digital-0.1-21.fc37.noarch
   dia-electric2-0.1-21.fc37.noarch
   dia-electronic-0.1-21.fc37.noarch
   electric
   emacs-vregs-mode-1.470-30.fc37.noarch
   espresso-ab-1.0-25.fc37.aarch64
   flterm-1.2-20.fc37.aarch64
   freeDiameter-1.5.0-5.fc37.aarch64
   fritzing-0.9.10-2.20220514.fc37.aarch64
   gerbv-2.9.2-2.fc37.aarch64
   ghc-chalmers-lava2000-devel
   ghdl-0.38~dev-16.20201208git83dfd49.fc37.aarch64
   gnucap-0.35-36.fc37.aarch64
   gnuradio-3.10.3.0-4.fc37.aarch64
   gnusim8085-1.4.1-5.fc37.aarch64
   gpsim-0.31.0-7.fc37.aarch64
   gputils-1.5.0-10.fc37.aarch64
   gr-osmosdr-0.2.3-30.20210217gita100eb02.fc37.aarch64
   gsim85-0.3-29.fc37.aarch64
   gspiceui
   gtkterm-1.2.1-2.fc37.aarch64
   gtkwave-3.3.113-1.fc37.aarch64
   hct-0.7.60-35.fc37.noarch
   hiredis-1.0.2-3.fc37.aarch64
   icaro-2.0-11.fc37.noarch
   icestorm-0-0.24.20221006gita545498.fc37.aarch64
```

```
irsim-9.7.104-8.fc37.aarch64
iverilog-11.0-6.fc37.aarch64
kicad-1:6.0.9-3.fc37.aarch64
ktechlab-0.50.0-2.fc37.aarch64
linsmith-0.99.31-10.fc37.aarch64
magic-8.3.348-1.fc37.aarch64
magic-doc-8.3.348-1.fc37.aarch64
mcu8051ide
mot-adms-2.3.7-5.fc37.aarch64
netgen-1.3.7-44.fc37.aarch64
nextpnr-1-14.20221109gitac17c36.fc37.aarch64
ngspice-38-1.fc37.aarch64
openocd-0.11.0-2.fc36.1.aarch64
pcb-4.2.0-10.fc37.aarch64
perl-Hardware-Verilog-Parser-0.13-40.fc37.noarch
perl-Hardware-Vhdl-Lexer-1.00-41.fc37.noarch
perl-Hardware-Vhdl-Parser-0.12-41.fc37.noarch
perl-Hardware-Vhdl-Tidy
perl-ModelSim-List-0.06-39.fc37.noarch
perl-Perlilog-1.0-20.fc37.noarch
perl-SystemC-Vregs-1.470-30.fc37.noarch
perl-Verilog-CodeGen
perl-Verilog-Perl-3.480-1.fc37.aarch64
perl-Verilog-Readmem-0.05-21.fc37.noarch
picocom-3.1-12.fc37.aarch64
pulseview-0.4.2-12.fc37.aarch64
python3-migen-0.9.2-16.20221006git639e66f.fc37.noarch
python3-myhdl-0.11-9.fc37.noarch
qucs-0.0.20~rc2-2.fc37.aarch64
rtl-sdr-0.6.0-12.fc37.aarch64
sdcc-4.1.0-4.fc37.aarch64
sigrok-cli-0.7.2-4.fc37.aarch64
sigrok-firmware-fx2lafw-0.1.7-7.fc37.noarch
smartsim-1.4-19.fc37.aarch64
srecord-1.64-23.fc37.aarch64
tclspice-38-1.fc37.aarch64
tkcvs-8.2.3-16.fc37.noarch
tkgate-2.0-37.beta10.fc37.aarch64
toped-0.9.81-32.svn2211.fc37.aarch64
trellis-1.2.1-12.20221109git35f5aff.fc37.aarch64
uisp-20050207-32.fc37.aarch64
verilator-4.226-1.fc37.aarch64
vhd2vl-2.5-15.fc37.aarch64
vrq
xcircuit-3.10.30-5.fc37.aarch64
xorg-x11-fonts-100dpi-7.5-34.fc37.noarch
xorg-x11-fonts-ISO8859-1-100dpi-7.5-34.fc37.noarch
xorg-x11-fonts-ISO8859-9-100dpi-7.5-34.fc37.noarch
xorg-x11-fonts-Type1-7.5-34.fc37.noarch
yosys-0.23-1.20221109gitc75f12a.fc37.aarch64
```

```
 Optional Packages:
   kdesvn-2.1.0-6.fc37.aarch64
   minicom-2.8-2.fc37.aarch64
[mydev@fedora /]$
```

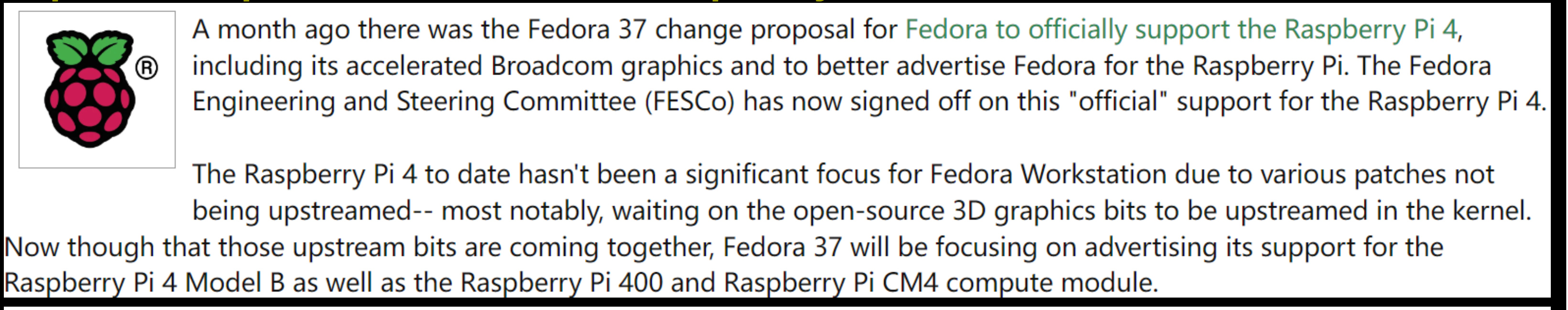
- sudo dnf install libevent libevent-devel boost boost-devel verilator
  yosys z3 z3-devel z3-libs java-z3 python-z3
- sudo dnf install tox python3-pytest python3-scapy python3-jinja2
  dfu-util libftdi libftdi-devel python3-libftdi python3-pyftdi
- ...

3.1.1.2 Fedora 37

- https://fedoraproject.org/wiki/Releases/37/ChangeSet
- https://www.phoronix.com/news/Fedora-37-Released

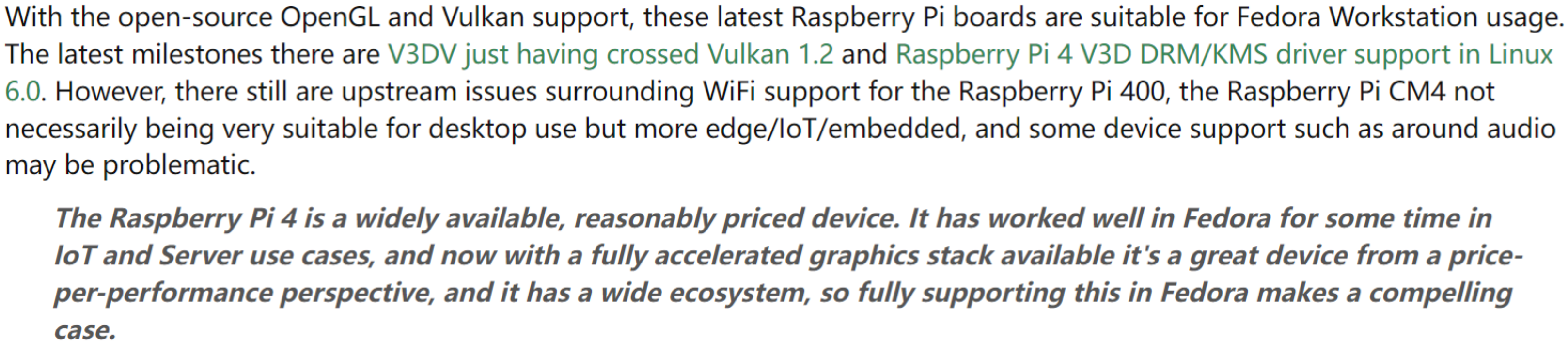
Raspberry Pi 4

- **Fedora 37 To Offer Official Support On Raspberry Pi 4 Devices**
  https://www.phoronix.com/news/Raspberry-Pi-4-Fedora-37



A month ago there was the Fedora 37 change proposal for Fedora to officially support the Raspberry Pi 4, including its accelerated Broadcom graphics and to better advertise Fedora for the Raspberry Pi. The Fedora Engineering and Steering Committee (FESCo) has now signed off on this "official" support for the Raspberry Pi 4.

The Raspberry Pi 4 to date hasn't been a significant focus for Fedora Workstation due to various patches not being upstreamed-- most notably, waiting on the open-source 3D graphics bits to be upstreamed in the kernel. Now though that those upstream bits are coming together, Fedora 37 will be focusing on advertising its support for the Raspberry Pi 4 Model B as well as the Raspberry Pi 400 and Raspberry Pi CM4 compute module.



With the open-source OpenGL and Vulkan support, these latest Raspberry Pi boards are suitable for Fedora Workstation usage. The latest milestones there are V3DV just having crossed Vulkan 1.2 and Raspberry Pi 4 V3D DRM/KMS driver support in Linux 6.0. However, there still are upstream issues surrounding WiFi support for the Raspberry Pi 400, the Raspberry Pi CM4 not necessarily being very suitable for desktop use but more edge/IoT/embedded, and some device support such as around audio may be problematic.

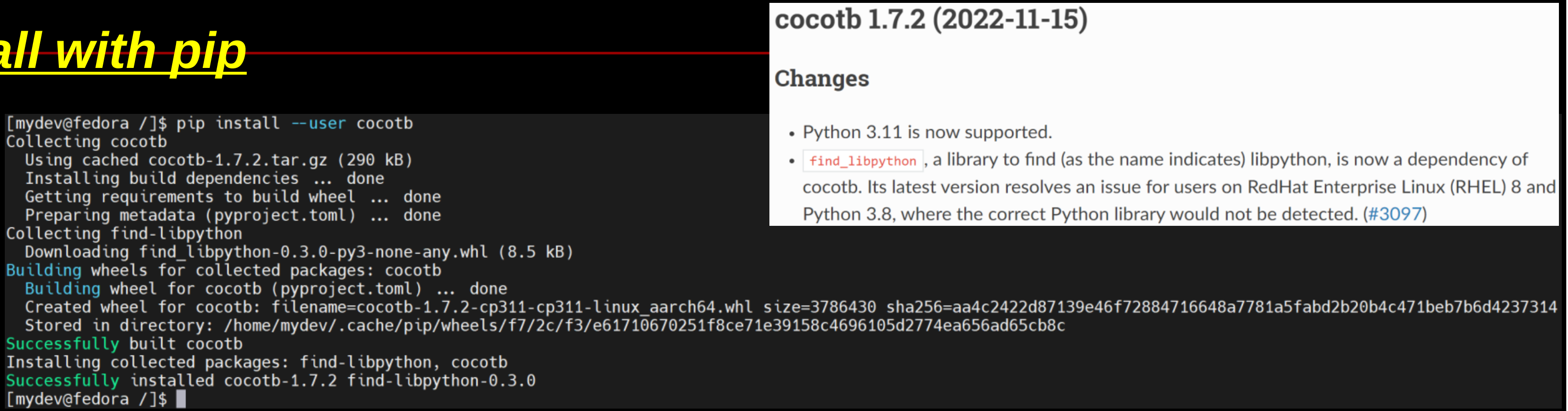
> ***The Raspberry Pi 4 is a widely available, reasonably priced device. It has worked well in Fedora for some time in IoT and Server use cases, and now with a fully accelerated graphics stack available it's a great device from a price-per-performance perspective, and it has a wide ecosystem, so fully supporting this in Fedora makes a compelling case.***

3.1.2 Cocotb

3.1.2.1 Installation

- https://docs.cocotb.org/en/stable/install.html

Install with pip



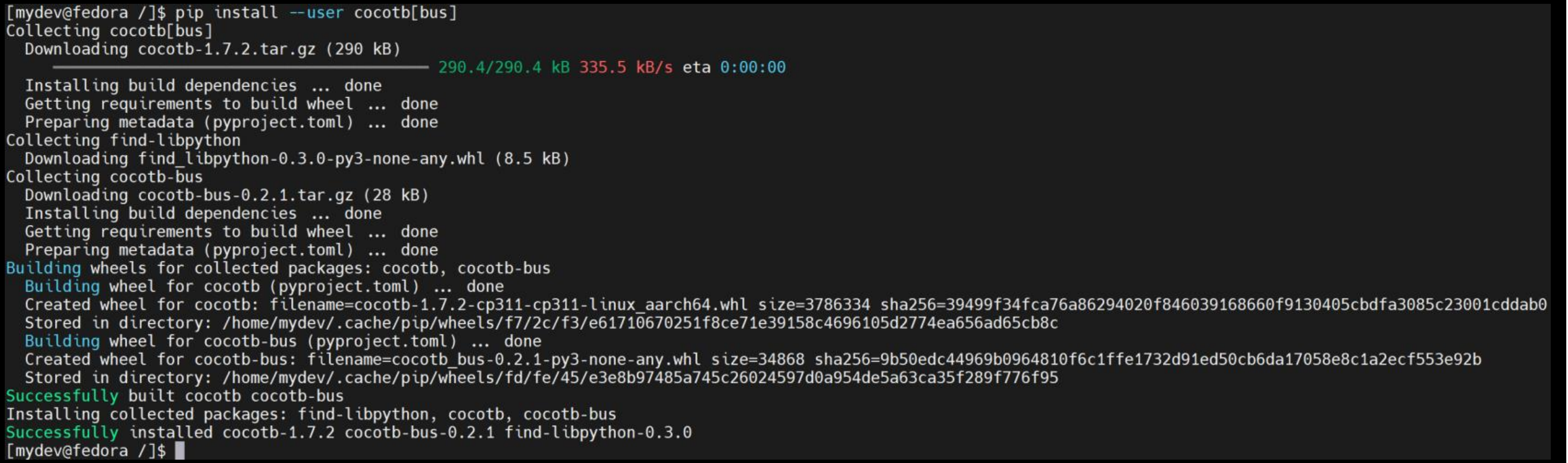
```
[mydev@fedora /]$ pip install --user cocotb
Collecting cocotb
  Using cached cocotb-1.7.2.tar.gz (290 kB)
  Installing build dependencies ... done
  Getting requirements to build wheel ... done
  Preparing metadata (pyproject.toml) ... done
Collecting find-libpython
  Downloading find_libpython-0.3.0-py3-none-any.whl (8.5 kB)
Building wheels for collected packages: cocotb
  Building wheel for cocotb (pyproject.toml) ... done
  Created wheel for cocotb: filename=cocotb-1.7.2-cp311-cp311-linux_aarch64.whl size=3786430 sha256=aa4c2422d87139e46f72884716648a7781a5fabd2b20b4c471beb7b6d4237314
  Stored in directory: /home/mydev/.cache/pip/wheels/f7/2c/f3/e61710670251f8ce71e39158c4696105d2774ea656ad65cb8c
Successfully built cocotb
Installing collected packages: find-libpython, cocotb
Successfully installed cocotb-1.7.2 find-libpython-0.3.0
[mydev@fedora /]$ 
```

cocotb 1.7.2 (2022-11-15)

Changes

- Python 3.11 is now supported.
- `find_libpython`, a library to find (as the name indicates) libpython, is now a dependency of cocotb. Its latest version resolves an issue for users on RedHat Enterprise Linux (RHEL) 8 and Python 3.8, where the correct Python library would not be detected. (#3097)

or

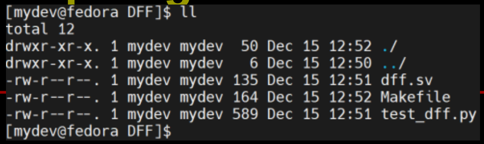


```
[mydev@fedora /]$ pip install --user cocotb[bus]
Collecting cocotb[bus]
  Downloading cocotb-1.7.2.tar.gz (290 kB)
     ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 290.4/290.4 kB 335.5 kB/s eta 0:00:00
  Installing build dependencies ... done
  Getting requirements to build wheel ... done
  Preparing metadata (pyproject.toml) ... done
Collecting find-libpython
  Downloading find_libpython-0.3.0-py3-none-any.whl (8.5 kB)
Collecting cocotb-bus
  Downloading cocotb-bus-0.2.1.tar.gz (28 kB)
  Installing build dependencies ... done
  Getting requirements to build wheel ... done
  Preparing metadata (pyproject.toml) ... done
Building wheels for collected packages: cocotb, cocotb-bus
  Building wheel for cocotb (pyproject.toml) ... done
  Created wheel for cocotb: filename=cocotb-1.7.2-cp311-cp311-linux_aarch64.whl size=3786334 sha256=39499f34fca76a86294020f846039168660f9130405cbdfa3085c23001cddab0
  Stored in directory: /home/mydev/.cache/pip/wheels/f7/2c/f3/e61710670251f8ce71e39158c4696105d2774ea656ad65cb8c
  Building wheel for cocotb-bus (pyproject.toml) ... done
  Created wheel for cocotb-bus: filename=cocotb_bus-0.2.1-py3-none-any.whl size=34868 sha256=9b50edc44969b0964810f6c1ffe1732d91ed50cb6da17058e8c1a2ecf553e92b
  Stored in directory: /home/mydev/.cache/pip/wheels/fd/fe/45/e3e8b97485a745c26024597d0a954de5a63ca35f289f776f95
Successfully built cocotb cocotb-bus
Installing collected packages: find-libpython, cocotb, cocotb-bus
Successfully installed cocotb-1.7.2 cocotb-bus-0.2.1 find-libpython-0.3.0
[mydev@fedora /]$ 
```

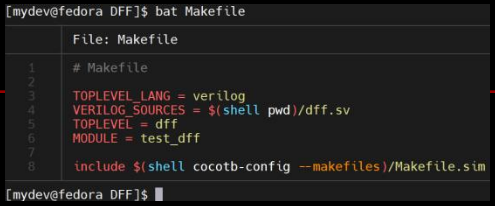
3.1.2.2 Usage

A simple D flip-flop on RPi4

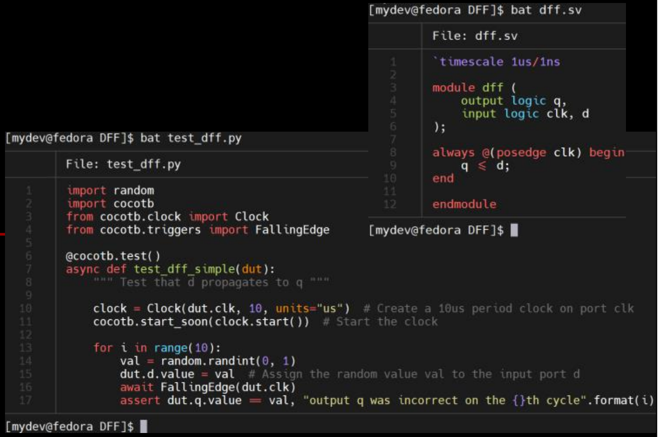
- https://github.com/cocotb/cocotb



```
[mydev@fedora DFF]$ ll
total 12
drwxr-xr-x. 1 mydev mydev  50 Dec 15 12:52 ./
drwxr-xr-x. 1 mydev mydev   6 Dec 15 12:50 ../
-rw-r--r--. 1 mydev mydev 135 Dec 15 12:51 dff.sv
-rw-r--r--. 1 mydev mydev 164 Dec 15 12:52 Makefile
-rw-r--r--. 1 mydev mydev 589 Dec 15 12:51 test_dff.py
[mydev@fedora DFF]$
```

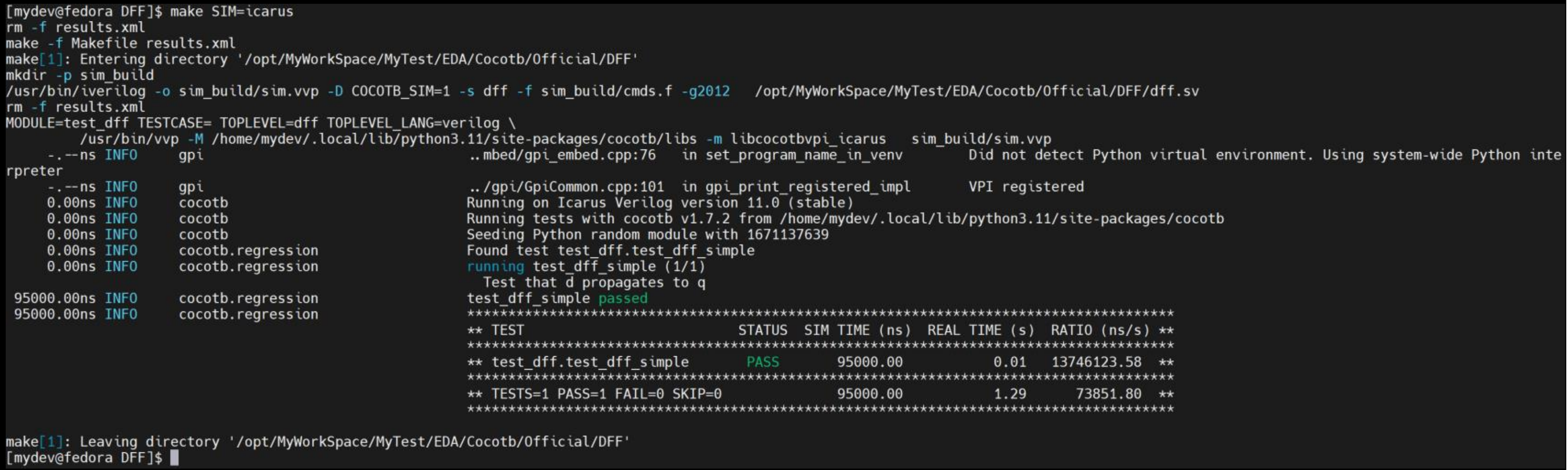


```
[mydev@fedora DFF]$ bat Makefile
File: Makefile
# Makefile

TOPLEVEL_LANG = verilog
VERILOG_SOURCES = $(shell pwd)/dff.sv
TOPLEVEL = dff
MODULE = test_dff

include $(shell cocotb-config --makefiles)/Makefile.sim
[mydev@fedora DFF]$
```

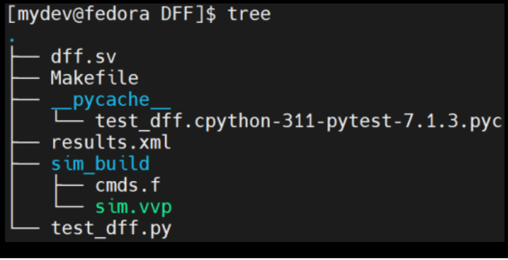


```
[mydev@fedora DFF]$ bat test_dff.py
File: test_dff.py
import random
import cocotb
from cocotb.clock import Clock
from cocotb.triggers import FallingEdge

@cocotb.test()
async def test_dff_simple(dut):
    """ Test that d propagates to q """

    clock = Clock(dut.clk, 10, units="us")  # Create a 10us period clock on port clk
    cocotb.start_soon(clock.start())  # Start the clock

    for i in range(10):
        val = random.randint(0, 1)
        dut.d.value = val  # Assign the random value val to the input port d
        await FallingEdge(dut.clk)
        assert dut.q.value == val, "output q was incorrect on the {}th cycle".format(i)
[mydev@fedora DFF]$
```

```
[mydev@fedora DFF]$ bat dff.sv
File: dff.sv
`timescale 1us/1ns

module dff (
    output logic q,
    input logic clk, d
);

always @(posedge clk) begin
    q <= d;
end

endmodule
[mydev@fedora DFF]$
```



```
[mydev@fedora DFF]$ make SIM=icarus
rm -f results.xml
make -f Makefile results.xml
make[1]: Entering directory '/opt/MyWorkSpace/MyTest/EDA/Cocotb/Official/DFF'
mkdir -p sim_build
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s dff -f sim_build/cmds.f -g2012   /opt/MyWorkSpace/MyTest/EDA/Cocotb/Official/DFF/dff.sv
rm -f results.xml
MODULE=test_dff TESTCASE= TOPLEVEL=dff TOPLEVEL_LANG=verilog \
         /usr/bin/vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:76   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python inte
rpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.7.2 from /home/mydev/.local/lib/python3.11/site-packages/cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1671137639
     0.00ns INFO     cocotb.regression                  Found test test_dff.test_dff_simple
     0.00ns INFO     cocotb.regression                  running test_dff_simple (1/1)
                                                          Test that d propagates to q
 95000.00ns INFO     cocotb.regression                  test_dff_simple passed
 95000.00ns INFO     cocotb.regression                  **************************************************************************************
                                                        ** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                        **************************************************************************************
                                                        ** test_dff.test_dff_simple       PASS        95000.00           0.01   13746123.58  **
                                                        **************************************************************************************
                                                        ** TESTS=1 PASS=1 FAIL=0 SKIP=0               95000.00           1.29      73851.80  **
                                                        **************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyTest/EDA/Cocotb/Official/DFF'
[mydev@fedora DFF]$
```



```
[mydev@fedora DFF]$ tree
.
├── dff.sv
├── Makefile
├── __pycache__
│   └── test_dff.cpython-311-pytest-7.1.3.pyc
├── results.xml
├── sim_build
│   ├── cmds.f
│   └── sim.vvp
└── test_dff.py
```

II. SpinalHDL with Cocotb on ARM

1) SpinalHDL

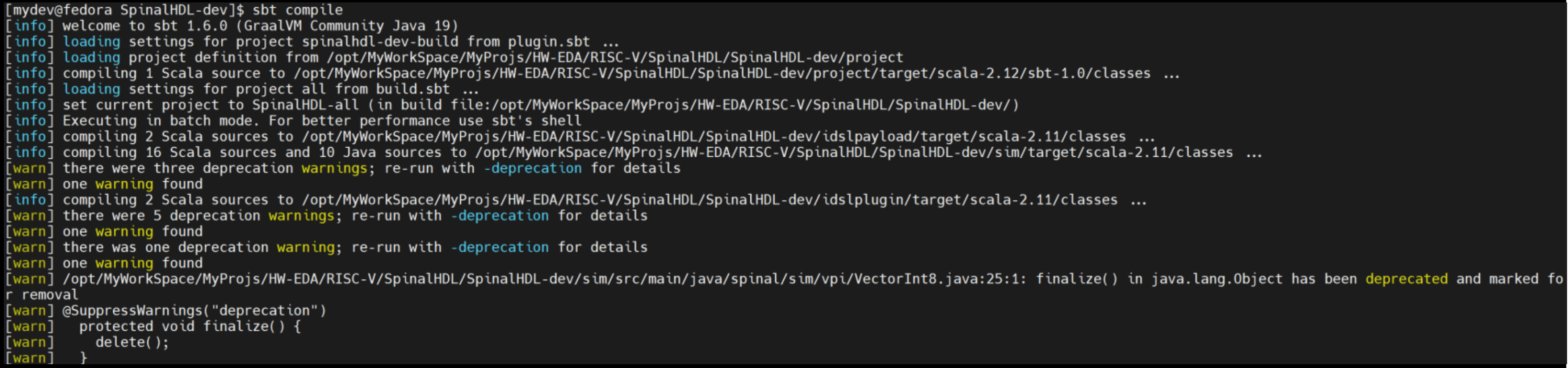
1.1 Test on RPi4

Tetralogy(env)

Code base:

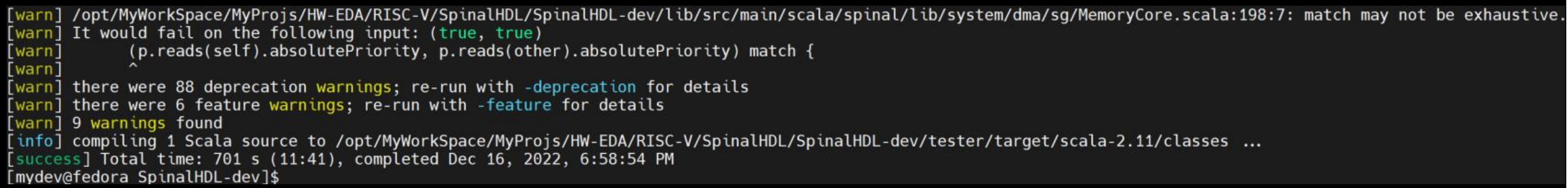
On dev branch, last commit: f518b561b4631c190dbd783ec02e46e2c7fbf8ff

- **Compile**



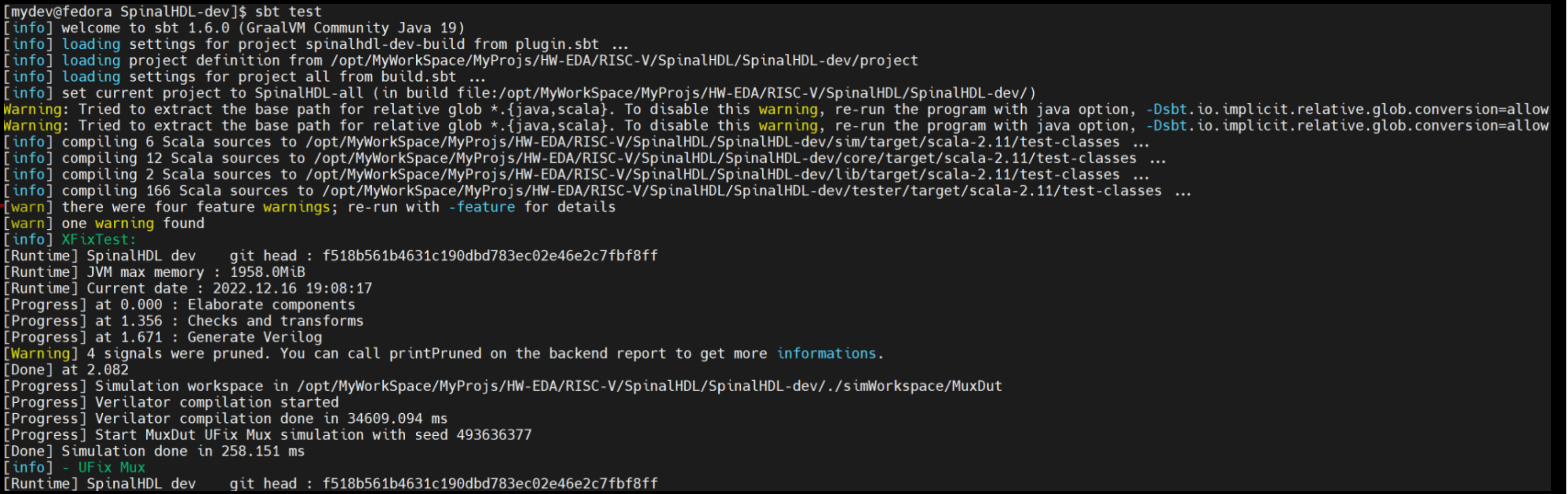
```
[mydev@fedora SpinalHDL-dev]$ sbt compile
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] compiling 1 Scala source to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project/target/scala-2.12/sbt-1.0/classes ...
[info] loading settings for project all from build.sbt ...
[info] set current project to SpinalHDL-all (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/)
[info] Executing in batch mode. For better performance use sbt's shell
[info] compiling 2 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslpayload/target/scala-2.11/classes ...
[info] compiling 16 Scala sources and 10 Java sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/sim/target/scala-2.11/classes ...
[warn] there were three deprecation warnings; re-run with -deprecation for details
[warn] one warning found
[info] compiling 2 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslplugin/target/scala-2.11/classes ...
[warn] there were 5 deprecation warnings; re-run with -deprecation for details
[warn] one warning found
[warn] there was one deprecation warning; re-run with -deprecation for details
[warn] one warning found
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/sim/src/main/java/spinal/sim/vpi/VectorInt8.java:25:1: finalize() in java.lang.Object has been deprecated and marked fo
r removal
[warn] @SuppressWarnings("deprecation")
[warn]   protected void finalize() {
[warn]     delete();
[warn]   }
```

...



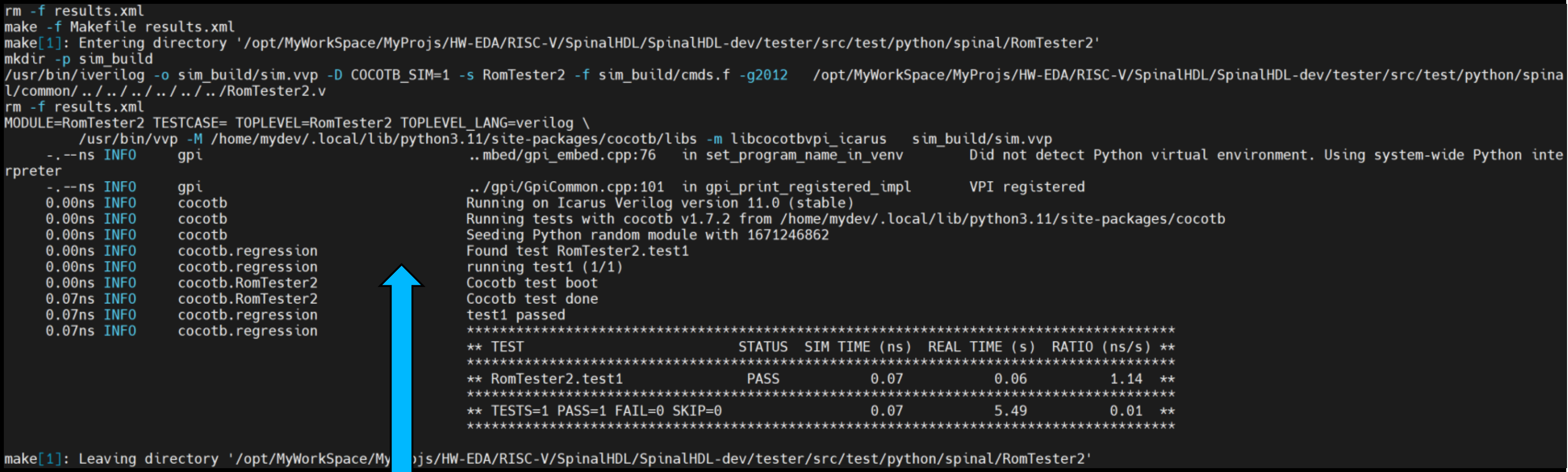
```
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/src/main/scala/spinal/lib/system/dma/sg/MemoryCore.scala:198:7: match may not be exhaustive.
[warn] It would fail on the following input: (true, true)
[warn]       (p.reads(self).absolutePriority, p.reads(other).absolutePriority) match {
[warn]       ^
[warn] there were 88 deprecation warnings; re-run with -deprecation for details
[warn] there were 6 feature warnings; re-run with -feature for details
[warn] 9 warnings found
[info] compiling 1 Scala source to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/target/scala-2.11/classes ...
[success] Total time: 701 s (11:41), completed Dec 16, 2022, 6:58:54 PM
[mydev@fedora SpinalHDL-dev]$
```

Test



```
[mydev@fedora SpinalHDL-dev]$ sbt test
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] loading settings for project all from build.sbt ...
[info] set current project to SpinalHDL-all (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/)
Warning: Tried to extract the base path for relative glob *.{java,scala}. To disable this warning, re-run the program with java option, -Dsbt.io.implicit.relative.glob.conversion=allow
Warning: Tried to extract the base path for relative glob *.{java,scala}. To disable this warning, re-run the program with java option, -Dsbt.io.implicit.relative.glob.conversion=allow
[info] compiling 6 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/sim/target/scala-2.11/test-classes ...
[info] compiling 12 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/core/target/scala-2.11/test-classes ...
[info] compiling 2 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/target/scala-2.11/test-classes ...
[info] compiling 166 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/target/scala-2.11/test-classes ...
[warn] there were four feature warnings; re-run with -feature for details
[warn] one warning found
[info] XFixTest:
[Runtime] SpinalHDL dev    git head : f518b561b4631c190dbd783ec02e46e2c7fbf8ff
[Runtime] JVM max memory : 1958.0MiB
[Runtime] Current date : 2022.12.16 19:08:17
[Progress] at 0.000 : Elaborate components
[Progress] at 1.356 : Checks and transforms
[Progress] at 1.671 : Generate Verilog
[Warning] 4 signals were pruned. You can call printPruned on the backend report to get more informations.
[Done] at 2.082
[Progress] Simulation workspace in /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/MuxDut
[Progress] Verilator compilation started
[Progress] Verilator compilation done in 34609.094 ms
[Progress] Start MuxDut UFix Mux simulation with seed 493636377
[Done] Simulation done in 258.151 ms
[info] - UFix Mux
[Runtime] SpinalHDL dev    git head : f518b561b4631c190dbd783ec02e46e2c7fbf8ff
```

...

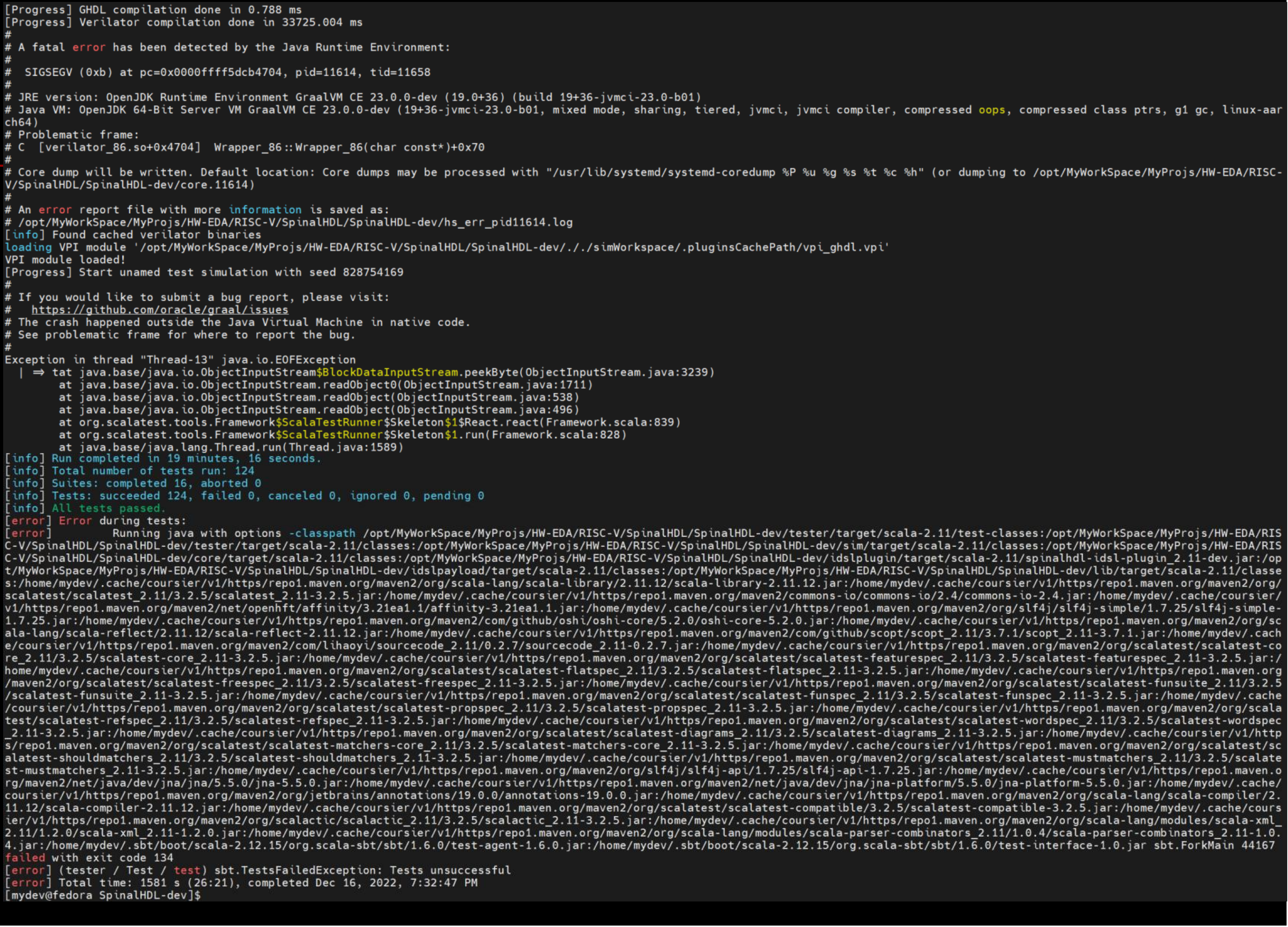


```
rm -f results.xml
make -f Makefile results.xml
make[1]: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/RomTester2'
mkdir -p sim_build
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s RomTester2 -f sim_build/cmds.f -g2012   /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spina
l/common/../../../../../../RomTester2.v
rm -f results.xml
MODULE=RomTester2 TESTCASE= TOPLEVEL=RomTester2 TOPLEVEL_LANG=verilog \
        /usr/bin/vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:76   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python inte
rpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.7.2 from /home/mydev/.local/lib/python3.11/site-packages/cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1671246862
     0.00ns INFO     cocotb.regression                  Found test RomTester2.test1
     0.00ns INFO     cocotb.regression                  running test1 (1/1)
     0.00ns INFO     cocotb.RomTester2                  Cocotb test boot
     0.07ns INFO     cocotb.RomTester2                  Cocotb test done
     0.07ns INFO     cocotb.regression                  test1 passed
     0.07ns INFO     cocotb.regression                  **************************************************************************************
                                                        ** TEST                         STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                        **************************************************************************************
                                                        ** RomTester2.test1              PASS           0.07           0.06          1.14  **
                                                        **************************************************************************************
                                                        ** TESTS=1 PASS=1 FAIL=0 SKIP=0                 0.07           5.49          0.01  **
                                                        **************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/RomTester2'
```

...

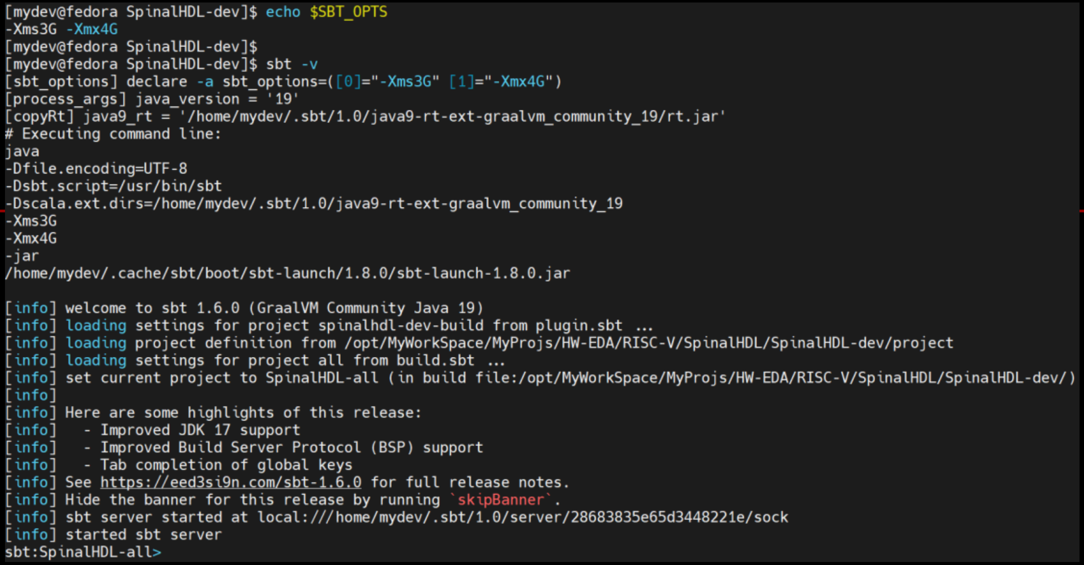
Cocotb is here

Meet a Coredump caused by out of memory in GraalVM and aborted:



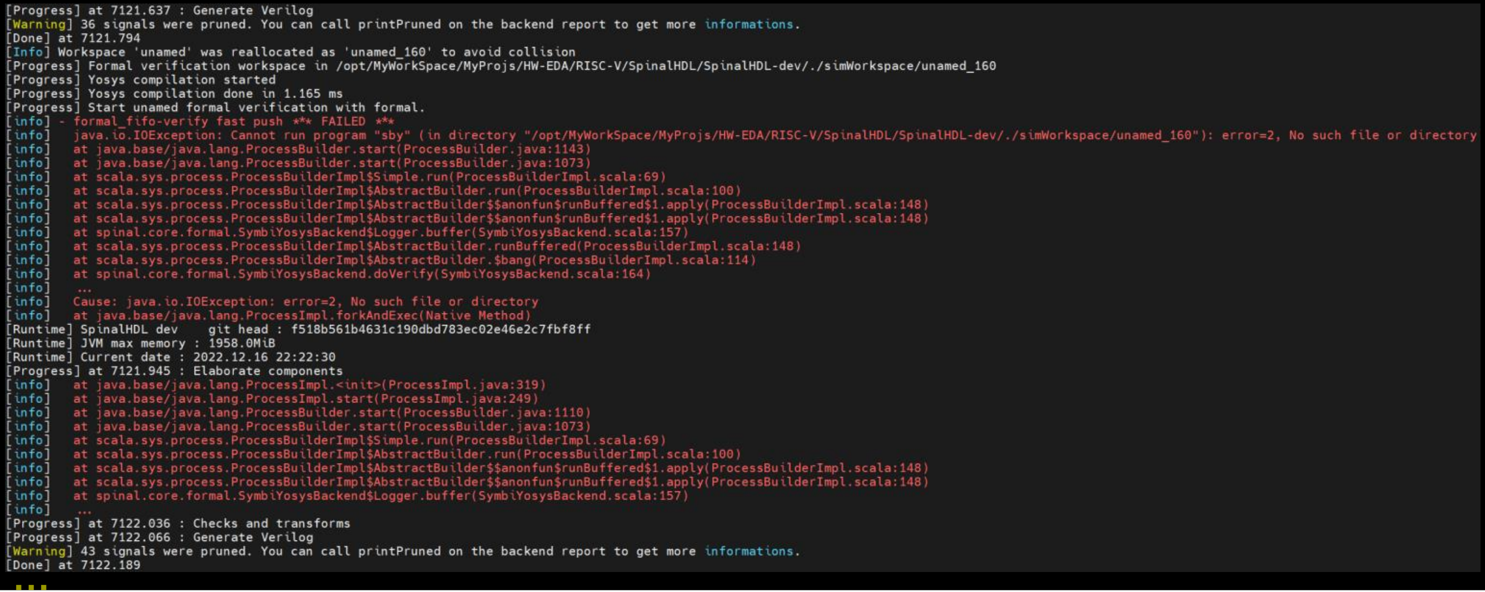
```
[Progress] GHDL compilation done in 0.788 ms
[Progress] Verilator compilation done in 33725.004 ms
#
# A fatal error has been detected by the Java Runtime Environment:
#
#  SIGSEGV (0xb) at pc=0x0000ffff5dcb4704, pid=11614, tid=11658
#
# JRE version: OpenJDK Runtime Environment GraalVM CE 23.0.0-dev (19.0+36) (build 19+36-jvmci-23.0-b01)
# Java VM: OpenJDK 64-Bit Server VM GraalVM CE 23.0.0-dev (19+36-jvmci-23.0-b01, mixed mode, sharing, tiered, jvmci, jvmci compiler, compressed oops, compressed class ptrs, g1 gc, linux-aar
ch64)
# Problematic frame:
# C  [verilator_86.so+0x4704]  Wrapper_86::Wrapper_86(char const*)+0x70
#
# Core dump will be written. Default location: Core dumps may be processed with "/usr/lib/systemd/systemd-coredump %P %u %g %s %t %c %h" (or dumping to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-
V/SpinalHDL/SpinalHDL-dev/core.11614)
#
# An error report file with more information is saved as:
# /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/hs_err_pid11614.log
[info] Found cached verilator binaries
loading VPI module '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/././simWorkspace/.pluginsCachePath/vpi_ghdl.vpi'
VPI module loaded!
[Progress] Start unamed test simulation with seed 828754169
#
# If you would like to submit a bug report, please visit:
#   https://github.com/oracle/graal/issues
# The crash happened outside the Java Virtual Machine in native code.
# See problematic frame for where to report the bug.
#
Exception in thread "Thread-13" java.io.EOFException
  | ⇒ tat java.base/java.io.ObjectInputStream$BlockDataInputStream.peekByte(ObjectInputStream.java:3239)
        at java.base/java.io.ObjectInputStream.readObject0(ObjectInputStream.java:1711)
        at java.base/java.io.ObjectInputStream.readObject(ObjectInputStream.java:538)
        at java.base/java.io.ObjectInputStream.readObject(ObjectInputStream.java:496)
        at org.scalatest.tools.Framework$ScalaTestRunner$Skeleton$1$React.react(Framework.scala:839)
        at org.scalatest.tools.Framework$ScalaTestRunner$Skeleton$1.run(Framework.scala:828)
        at java.base/java.lang.Thread.run(Thread.java:1589)
[info] Run completed in 19 minutes, 16 seconds.
[info] Total number of tests run: 124
[info] Suites: completed 16, aborted 0
[info] Tests: succeeded 124, failed 0, canceled 0, ignored 0, pending 0
[info] All tests passed.
[error] Error during tests:
[error]         Running java with options -classpath /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/target/scala-2.11/test-classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RIS
C-V/SpinalHDL/SpinalHDL-dev/tester/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/sim/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RIS
C-V/SpinalHDL/SpinalHDL-dev/core/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslplugin/target/scala-2.11/spinalhdl-idsl-plugin_2.11-dev.jar:/op
t/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslpayload/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/target/scala-2.11/classe
s:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scala-library/2.11.12/scala-library-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/
scalatest/scalatest_2.11/3.2.5/scalatest_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/commons-io/commons-io/2.4/commons-io-2.4.jar:/home/mydev/.cache/coursier/
v1/https/repo1.maven.org/maven2/net/openhft/affinity/3.21ea1.1/affinity-3.21ea1.1.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/slf4j/slf4j-simple/1.7.25/slf4j-simple-
1.7.25.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/github/oshi/oshi-core/5.2.0/oshi-core-5.2.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/sc
ala-lang/scala-reflect/2.11.12/scala-reflect-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/github/scopt/scopt_2.11/3.7.1/scopt_2.11-3.7.1.jar:/home/mydev/.cach
e/coursier/v1/https/repo1.maven.org/maven2/com/lihaoyi/sourcecode_2.11/0.2.7/sourcecode_2.11-0.2.7.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-co
re_2.11/3.2.5/scalatest-core_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-featurespec_2.11/3.2.5/scalatest-featurespec_2.11-3.2.5.jar:/
home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-flatspec_2.11/3.2.5/scalatest-flatspec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org
/maven2/org/scalatest/scalatest-freespec_2.11/3.2.5/scalatest-freespec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-funsuite_2.11/3.2.5
/scalatest-funsuite_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-funspec_2.11/3.2.5/scalatest-funspec_2.11-3.2.5.jar:/home/mydev/.cache
/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-propspec_2.11/3.2.5/scalatest-propspec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala
test/scalatest-refspec_2.11/3.2.5/scalatest-refspec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-wordspec_2.11/3.2.5/scalatest-wordspec
_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-diagrams_2.11/3.2.5/scalatest-diagrams_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/http
s/repo1.maven.org/maven2/org/scalatest/scalatest-matchers-core_2.11/3.2.5/scalatest-matchers-core_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/sc
alatest-shouldmatchers_2.11/3.2.5/scalatest-shouldmatchers_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-mustmatchers_2.11/3.2.5/scalate
st-mustmatchers_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/slf4j/slf4j-api/1.7.25/slf4j-api-1.7.25.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.o
rg/maven2/net/java/dev/jna/jna/5.5.0/jna-5.5.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/net/java/dev/jna/jna-platform/5.5.0/jna-platform-5.5.0.jar:/home/mydev/.cache/
coursier/v1/https/repo1.maven.org/maven2/org/jetbrains/annotations/19.0.0/annotations-19.0.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scala-compiler/2.
11.12/scala-compiler-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-compatible/3.2.5/scalatest-compatible-3.2.5.jar:/home/mydev/.cache/cours
ier/v1/https/repo1.maven.org/maven2/org/scalactic/scalactic_2.11/3.2.5/scalactic_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/modules/scala-xml_
2.11/1.2.0/scala-xml_2.11-1.2.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/modules/scala-parser-combinators_2.11/1.0.4/scala-parser-combinators_2.11-1.0.
4.jar:/home/mydev/.sbt/boot/scala-2.12.15/org.scala-sbt/sbt/1.6.0/test-agent-1.6.0.jar:/home/mydev/.sbt/boot/scala-2.12.15/org.scala-sbt/sbt/1.6.0/test-interface-1.0.jar sbt.ForkMain 44167
failed with exit code 134
[error] (tester / Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 1581 s (26:21), completed Dec 16, 2022, 7:32:47 PM
[mydev@fedora SpinalHDL-dev]$
```

set env variable SBT_OPTS or JAVA_OPTS to "-Xms3G -Xmx4G" and retest:



```
[mydev@fedora SpinalHDL-dev]$ echo $SBT_OPTS
-Xms3G -Xmx4G
[mydev@fedora SpinalHDL-dev]$
[mydev@fedora SpinalHDL-dev]$ sbt -v
[sbt_options] declare -a sbt_options=([0]="-Xms3G" [1]="-Xmx4G")
[process_args] java_version = '19'
[copyRt] java9_rt = '/home/mydev/.sbt/1.0/java9-rt-ext-graalvm_community_19/rt.jar'
# Executing command line:
java
-Dfile.encoding=UTF-8
-Dsbt.script=/usr/bin/sbt
-Dscala.ext.dirs=/home/mydev/.sbt/1.0/java9-rt-ext-graalvm_community_19
-Xms3G
-Xmx4G
-jar
/home/mydev/.cache/sbt/boot/sbt-launch/1.8.0/sbt-launch-1.8.0.jar

[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] loading settings for project all from build.sbt ...
[info] set current project to SpinalHDL-all (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/)
[info]
[info] Here are some highlights of this release:
[info]   - Improved JDK 17 support
[info]   - Improved Build Server Protocol (BSP) support
[info]   - Tab completion of global keys
[info] See https://eed3si9n.com/sbt-1.6.0 for full release notes.
[info] Hide the banner for this release by running `skipBanner`.
[info] sbt server started at local:///home/mydev/.sbt/1.0/server/28683835e65d3448221e/sock
[info] started sbt server
sbt:SpinalHDL-all>
```

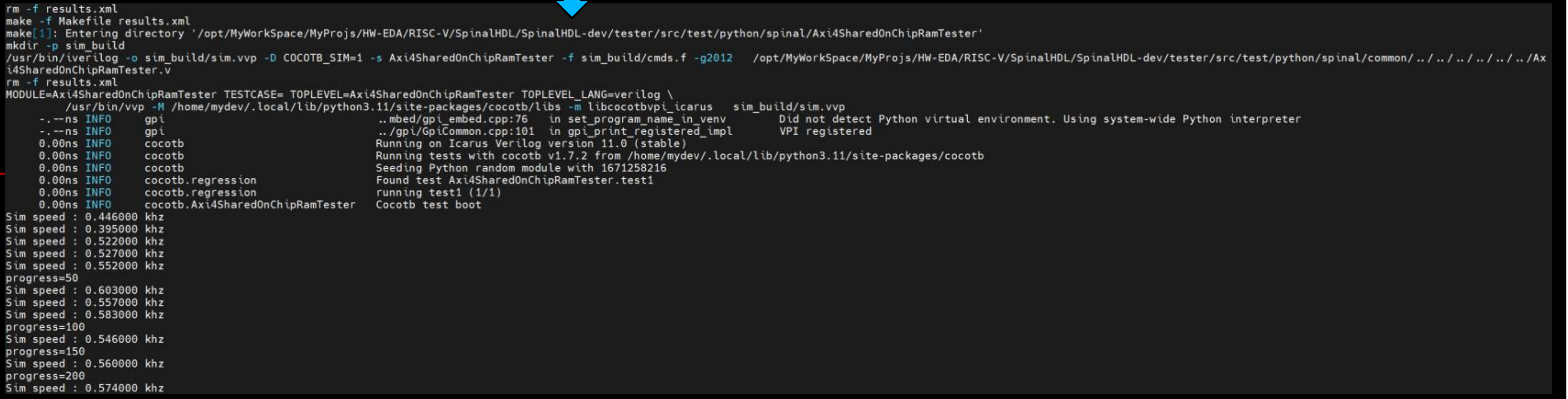
...



```
[Progress] at 7121.637 : Generate Verilog
[Warning] 36 signals were pruned. You can call printPruned on the backend report to get more informations.
[Done] at 7121.794
[Info] Workspace 'unamed' was reallocated as 'unamed_160' to avoid collision
[Progress] Formal verification workspace in /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/unamed_160
[Progress] Yosys compilation started
[Progress] Yosys compilation done in 1.165 ms
[Progress] Start unamed formal verification with formal.
[info] - formal_fifo-verify fast push *** FAILED ***
[info]   java.io.IOException: Cannot run program "sby" (in directory "/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/unamed_160"): error=2, No such file or directory
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1143)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:69)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:100)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at spinal.core.formal.SymbiYosysBackend$Logger.buffer(SymbiYosysBackend.scala:157)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.runBuffered(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.$bang(ProcessBuilderImpl.scala:114)
[info]   at spinal.core.formal.SymbiYosysBackend.doVerify(SymbiYosysBackend.scala:164)
[info]   ...
[info]   Cause: java.io.IOException: error=2, No such file or directory
[info]   at java.base/java.lang.ProcessImpl.forkAndExec(Native Method)
[Runtime] SpinalHDL dev    git head : f518b561b4631c190dbd783ec02e46e2c7fbf8ff
[Runtime] JVM max memory : 1958.0MiB
[Runtime] Current date : 2022.12.16 22:22:30
[Progress] at 7121.945 : Elaborate components
[info]   at java.base/java.lang.ProcessImpl.<init>(ProcessImpl.java:319)
[info]   at java.base/java.lang.ProcessImpl.start(ProcessImpl.java:249)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1110)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:69)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:100)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at spinal.core.formal.SymbiYosysBackend$Logger.buffer(SymbiYosysBackend.scala:157)
[info]   ...
[Progress] at 7122.036 : Checks and transforms
[Progress] at 7122.066 : Generate Verilog
[Warning] 43 signals were pruned. You can call printPruned on the backend report to get more informations.
[Done] at 7122.189
```

...

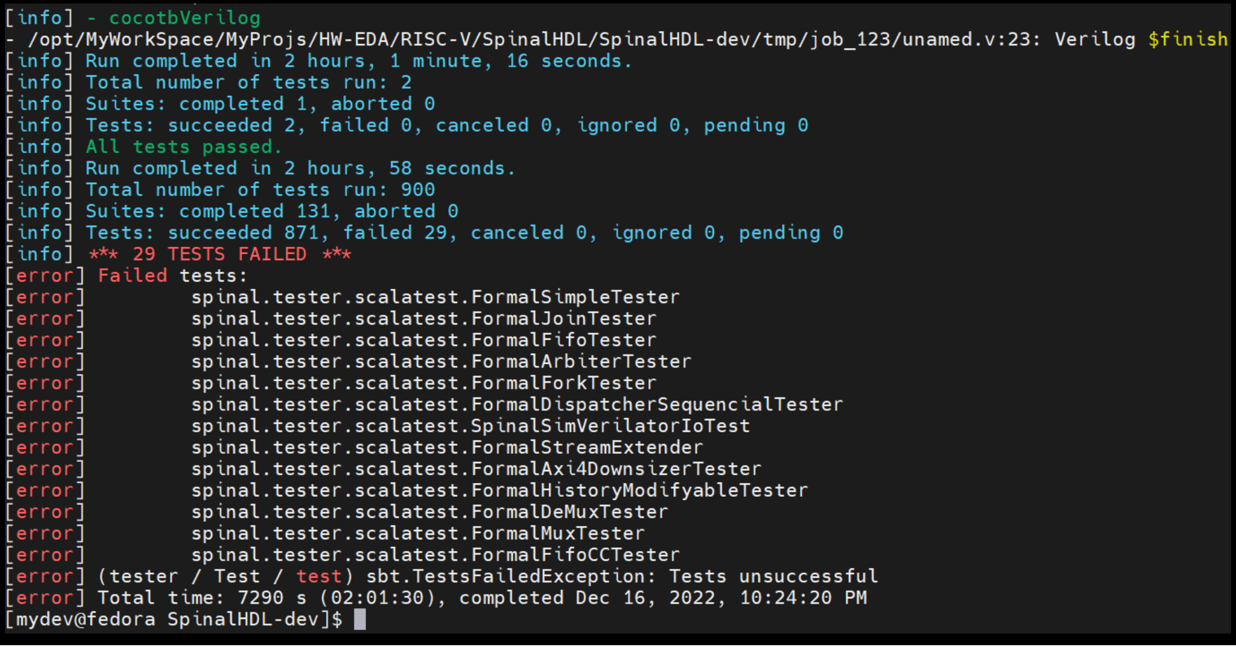
Cocotb is here



```
rm -f results.xml
make -f Makefile results.xml
make[1]: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester'
mkdir -p sim_build
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s Axi4SharedOnChipRamTester -f sim_build/cmds.f -g2012   /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/common/../../../../../../Ax
i4SharedOnChipRamTester.v
rm -f results.xml
MODULE=Axi4SharedOnChipRamTester TESTCASE= TOPLEVEL=Axi4SharedOnChipRamTester TOPLEVEL_LANG=verilog \
         /usr/bin/vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:76   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python interpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.7.2 from /home/mydev/.local/lib/python3.11/site-packages/cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1671258216
     0.00ns INFO     cocotb.regression                  Found test Axi4SharedOnChipRamTester.test1
     0.00ns INFO     cocotb.regression                  running test1 (1/1)
     0.00ns INFO     cocotb.Axi4SharedOnChipRamTester   Cocotb test boot
Sim speed : 0.446000 khz
Sim speed : 0.395000 khz
Sim speed : 0.522000 khz
Sim speed : 0.527000 khz
Sim speed : 0.552000 khz
progress=50
Sim speed : 0.603000 khz
Sim speed : 0.557000 khz
Sim speed : 0.583000 khz
progress=100
Sim speed : 0.546000 khz
progress=150
Sim speed : 0.560000 khz
progress=200
Sim speed : 0.574000 khz
```

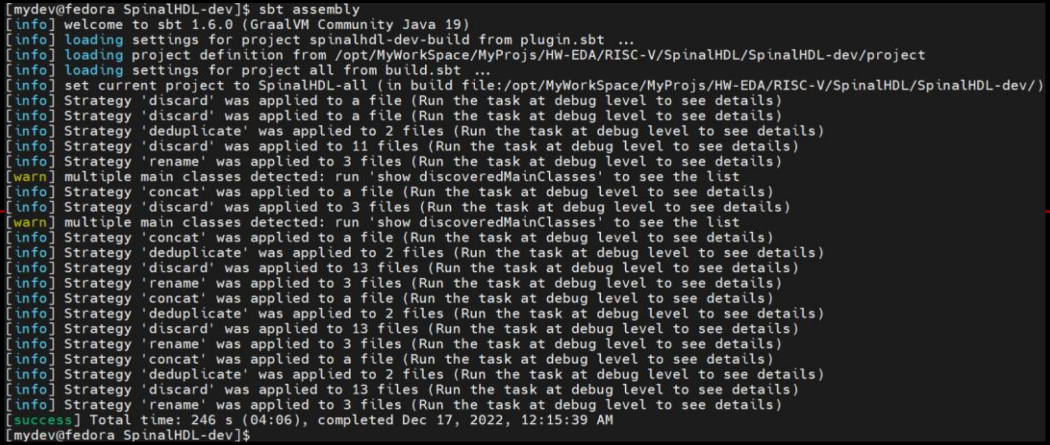
...

the final test result:



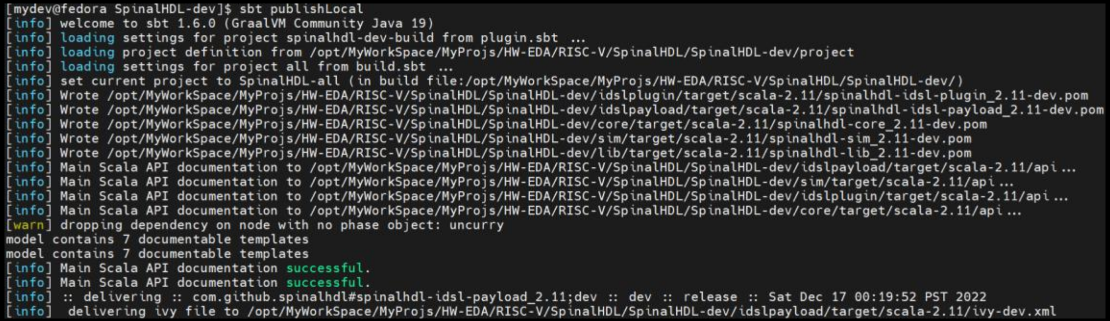
```
[info] - cocotbVerilog
- /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tmp/job_123/unamed.v:23: Verilog $finish
[info] Run completed in 2 hours, 1 minute, 16 seconds.
[info] Total number of tests run: 2
[info] Suites: completed 1, aborted 0
[info] Tests: succeeded 2, failed 0, canceled 0, ignored 0, pending 0
[info] All tests passed.
[info] Run completed in 2 hours, 58 seconds.
[info] Total number of tests run: 900
[info] Suites: completed 131, aborted 0
[info] Tests: succeeded 871, failed 29, canceled 0, ignored 0, pending 0
[info] *** 29 TESTS FAILED ***
[error] Failed tests:
[error]         spinal.tester.scalatest.FormalSimpleTester
[error]         spinal.tester.scalatest.FormalJoinTester
[error]         spinal.tester.scalatest.FormalFifoTester
[error]         spinal.tester.scalatest.FormalArbiterTester
[error]         spinal.tester.scalatest.FormalForkTester
[error]         spinal.tester.scalatest.FormalDispatcherSequencialTester
[error]         spinal.tester.scalatest.SpinalSimVerilatorIoTest
[error]         spinal.tester.scalatest.FormalStreamExtender
[error]         spinal.tester.scalatest.FormalAxi4DownsizerTester
[error]         spinal.tester.scalatest.FormalHistoryModifyableTester
[error]         spinal.tester.scalatest.FormalDeMuxTester
[error]         spinal.tester.scalatest.FormalMuxTester
[error]         spinal.tester.scalatest.FormalFifoCCTester
[error] (tester / Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 7290 s (02:01:30), completed Dec 16, 2022, 10:24:20 PM
[mydev@fedora SpinalHDL-dev]$ 
```

Assembly



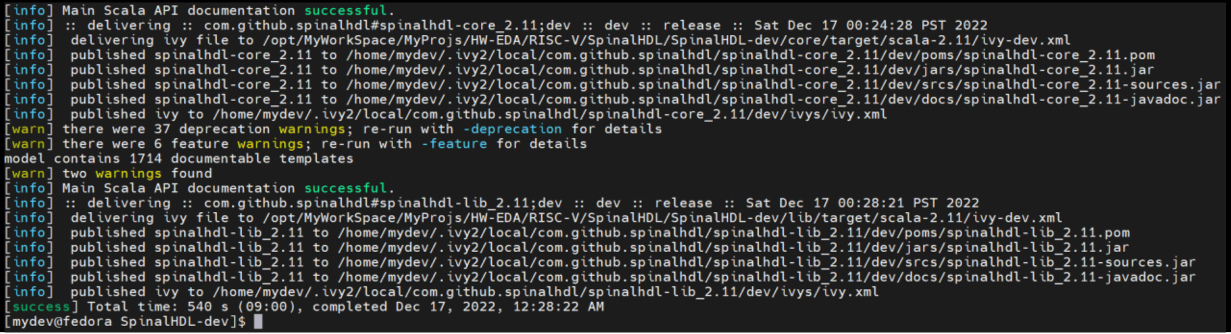
```
[mydev@fedora SpinalHDL-dev]$ sbt assembly
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] loading settings for project all from build.sbt ...
[info] set current project to SpinalHDL-all (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/)
[info] Strategy 'discard' was applied to a file (Run the task at debug level to see details)
[info] Strategy 'discard' was applied to a file (Run the task at debug level to see details)
[info] Strategy 'deduplicate' was applied to 2 files (Run the task at debug level to see details)
[info] Strategy 'discard' was applied to 11 files (Run the task at debug level to see details)
[info] Strategy 'rename' was applied to 3 files (Run the task at debug level to see details)
[warn] multiple main classes detected: run 'show discoveredMainClasses' to see the list
[info] Strategy 'concat' was applied to a file (Run the task at debug level to see details)
[info] Strategy 'discard' was applied to 3 files (Run the task at debug level to see details)
[warn] multiple main classes detected: run 'show discoveredMainClasses' to see the list
[info] Strategy 'concat' was applied to a file (Run the task at debug level to see details)
[info] Strategy 'deduplicate' was applied to 2 files (Run the task at debug level to see details)
[info] Strategy 'discard' was applied to 13 files (Run the task at debug level to see details)
[info] Strategy 'rename' was applied to 3 files (Run the task at debug level to see details)
[info] Strategy 'concat' was applied to a file (Run the task at debug level to see details)
[info] Strategy 'deduplicate' was applied to 2 files (Run the task at debug level to see details)
[info] Strategy 'discard' was applied to 13 files (Run the task at debug level to see details)
[info] Strategy 'rename' was applied to 3 files (Run the task at debug level to see details)
[info] Strategy 'concat' was applied to a file (Run the task at debug level to see details)
[info] Strategy 'deduplicate' was applied to 2 files (Run the task at debug level to see details)
[info] Strategy 'discard' was applied to 13 files (Run the task at debug level to see details)
[info] Strategy 'rename' was applied to 3 files (Run the task at debug level to see details)
[success] Total time: 246 s (04:06), completed Dec 17, 2022, 12:15:39 AM
[mydev@fedora SpinalHDL-dev]$
```

Publish



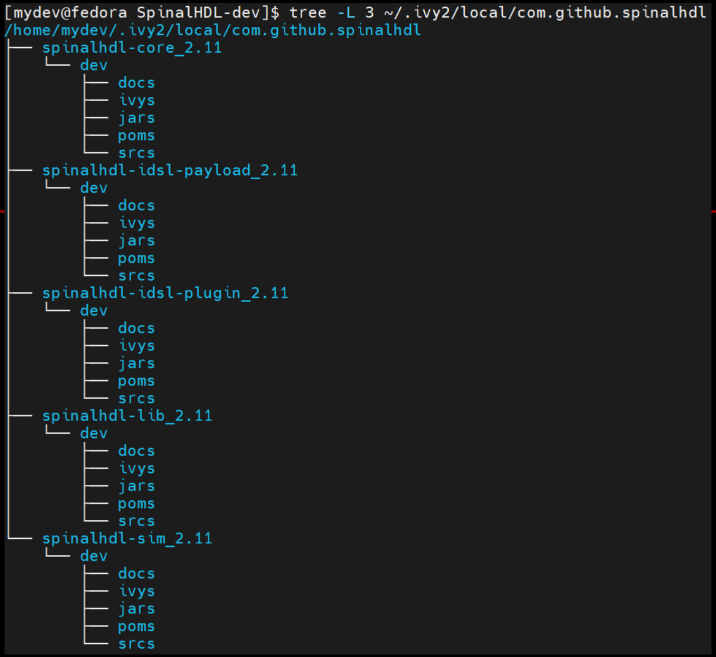
```
[mydev@fedora SpinalHDL-dev]$ sbt publishLocal
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] loading settings for project all from build.sbt ...
[info] set current project to SpinalHDL-all (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/)
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslplugin/target/scala-2.11/spinalhdl-idsl-plugin_2.11-dev.pom
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslpayload/target/scala-2.11/spinalhdl-idsl-payload_2.11-dev.pom
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/core/target/scala-2.11/spinalhdl-core_2.11-dev.pom
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/sim/target/scala-2.11/spinalhdl-sim_2.11-dev.pom
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/target/scala-2.11/spinalhdl-lib_2.11-dev.pom
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslpayload/target/scala-2.11/api...
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/sim/target/scala-2.11/api...
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslplugin/target/scala-2.11/api...
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/core/target/scala-2.11/api...
[warn] dropping dependency on node with no phase object: uncurry
model contains 7 documentable templates
model contains 7 documentable templates
[info] Main Scala API documentation successful.
[info] Main Scala API documentation successful.
[info] :: delivering :: com.github.spinalhdl#spinalhdl-idsl-payload_2.11;dev :: dev :: release :: Sat Dec 17 00:19:52 PST 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslpayload/target/scala-2.11/ivy-dev.xml
```

...

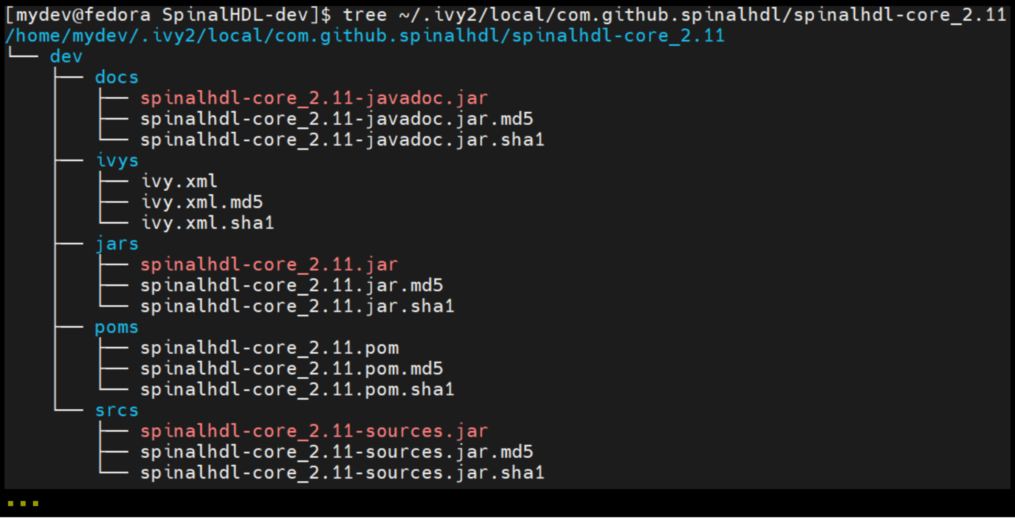


```
[info] Main Scala API documentation successful.
[info] :: delivering :: com.github.spinalhdl#spinalhdl-core_2.11;dev :: dev :: release :: Sat Dec 17 00:24:28 PST 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/core/target/scala-2.11/ivy-dev.xml
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/poms/spinalhdl-core_2.11.pom
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/jars/spinalhdl-core_2.11.jar
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/srcs/spinalhdl-core_2.11-sources.jar
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/docs/spinalhdl-core_2.11-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/ivys/ivy.xml
[warn] there were 37 deprecation warnings; re-run with -deprecation for details
[warn] there were 6 feature warnings; re-run with -feature for details
model contains 1714 documentable templates
[warn] two warnings found
[info] Main Scala API documentation successful.
[info] :: delivering :: com.github.spinalhdl#spinalhdl-lib_2.11;dev :: dev :: release :: Sat Dec 17 00:28:21 PST 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/target/scala-2.11/ivy-dev.xml
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/poms/spinalhdl-lib_2.11.pom
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/jars/spinalhdl-lib_2.11.jar
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/srcs/spinalhdl-lib_2.11-sources.jar
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/docs/spinalhdl-lib_2.11-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/ivys/ivy.xml
[success] Total time: 540 s (09:00), completed Dec 17, 2022, 12:28:22 AM
[mydev@fedora SpinalHDL-dev]$
```

check what’s in the ivy2 repository now:



```
[mydev@fedora SpinalHDL-dev]$ tree -L 3 ~/.ivy2/local/com.github.spinalhdl
/home/mydev/.ivy2/local/com.github.spinalhdl
├── spinalhdl-core_2.11
│   └── dev
│       ├── docs
│       ├── ivys
│       ├── jars
│       ├── poms
│       └── srcs
├── spinalhdl-idsl-payload_2.11
│   └── dev
│       ├── docs
│       ├── ivys
│       ├── jars
│       ├── poms
│       └── srcs
├── spinalhdl-idsl-plugin_2.11
│   └── dev
│       ├── docs
│       ├── ivys
│       ├── jars
│       ├── poms
│       └── srcs
├── spinalhdl-lib_2.11
│   └── dev
│       ├── docs
│       ├── ivys
│       ├── jars
│       ├── poms
│       └── srcs
└── spinalhdl-sim_2.11
    └── dev
        ├── docs
        ├── ivys
        ├── jars
        ├── poms
        └── srcs
```



```
[mydev@fedora SpinalHDL-dev]$ tree ~/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11
/home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11
└── dev
    ├── docs
    │   ├── spinalhdl-core_2.11-javadoc.jar
    │   ├── spinalhdl-core_2.11-javadoc.jar.md5
    │   └── spinalhdl-core_2.11-javadoc.jar.sha1
    ├── ivys
    │   ├── ivy.xml
    │   ├── ivy.xml.md5
    │   └── ivy.xml.sha1
    ├── jars
    │   ├── spinalhdl-core_2.11.jar
    │   ├── spinalhdl-core_2.11.jar.md5
    │   └── spinalhdl-core_2.11.jar.sha1
    ├── poms
    │   ├── spinalhdl-core_2.11.pom
    │   ├── spinalhdl-core_2.11.pom.md5
    │   └── spinalhdl-core_2.11.pom.sha1
    └── srcs
        ├── spinalhdl-core_2.11-sources.jar
        ├── spinalhdl-core_2.11-sources.jar.md5
        └── spinalhdl-core_2.11-sources.jar.sha1
```

...

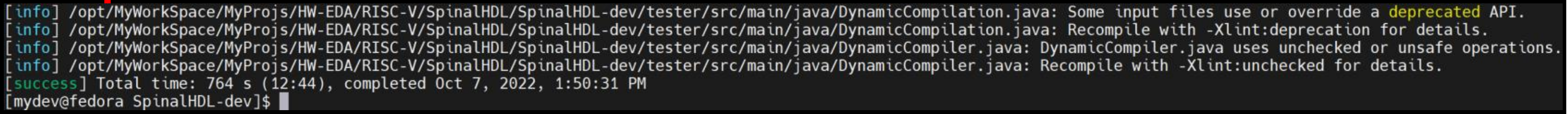
Tetralogy(old env in Oct, for comparison)

- For more details, you may refer to our previous talk "Hosting FOSS EDA tools for RISC-V cross-platform development on RPi4" at COSCon 2022(Online).

Code base:

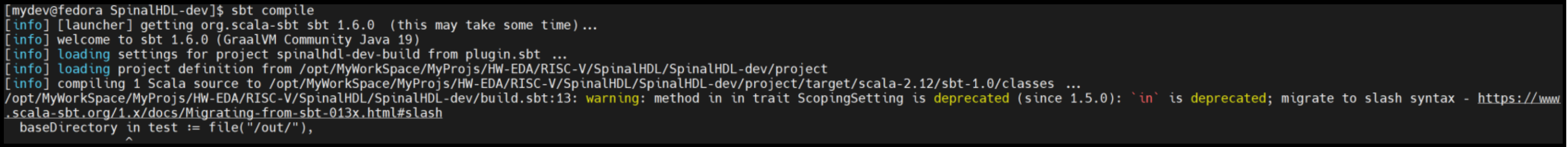
On dev branch, last commit: 530a200105546759f2650bd7c9c60fa468952dbe

- **Compile**



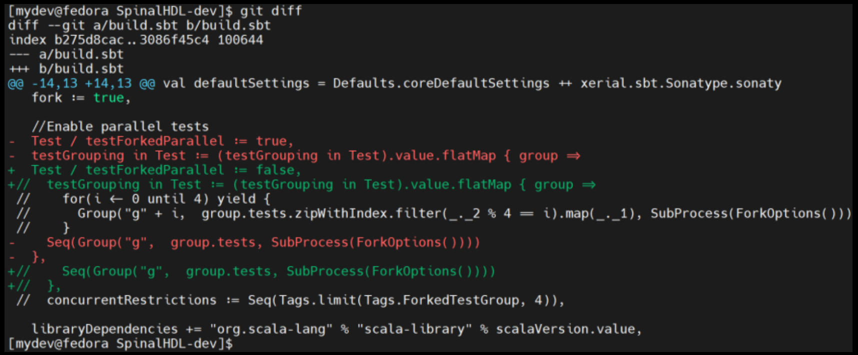
```
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/main/java/DynamicCompilation.java: Some input files use or override a deprecated API.
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/main/java/DynamicCompilation.java: Recompile with -Xlint:deprecation for details.
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/main/java/DynamicCompiler.java: DynamicCompiler.java uses unchecked or unsafe operations.
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/main/java/DynamicCompiler.java: Recompile with -Xlint:unchecked for details.
[success] Total time: 764 s (12:44), completed Oct 7, 2022, 1:50:31 PM
[mydev@fedora SpinalHDL-dev]$ █
```

...

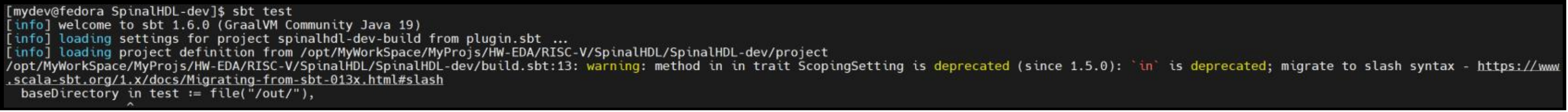


```
[mydev@fedora SpinalHDL-dev]$ sbt compile
[info] [launcher] getting org.scala-sbt sbt 1.6.0  (this may take some time)...
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] compiling 1 Scala source to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project/target/scala-2.12/sbt-1.0/classes ...
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/build.sbt:13: warning: method in in trait ScopingSetting is deprecated (since 1.5.0): `in` is deprecated; migrate to slash syntax - https://www
.scala-sbt.org/1.x/docs/Migrating-from-sbt-013x.html#slash
  baseDirectory in test := file("/out/"),
                ^
```

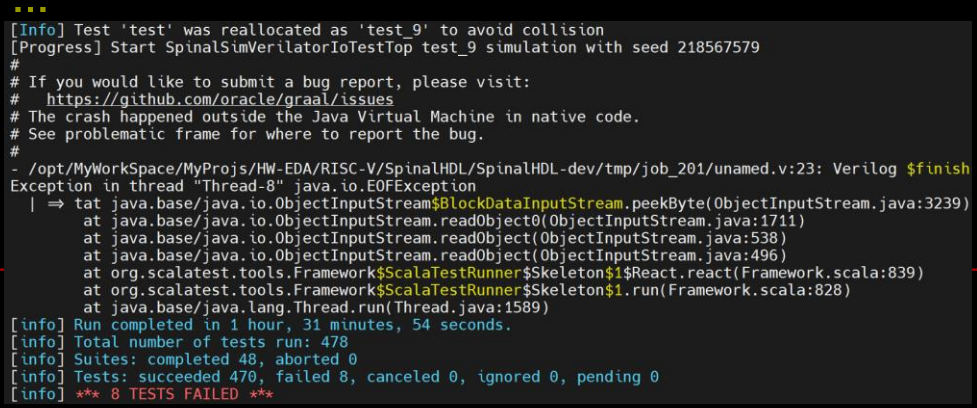
- **Test**



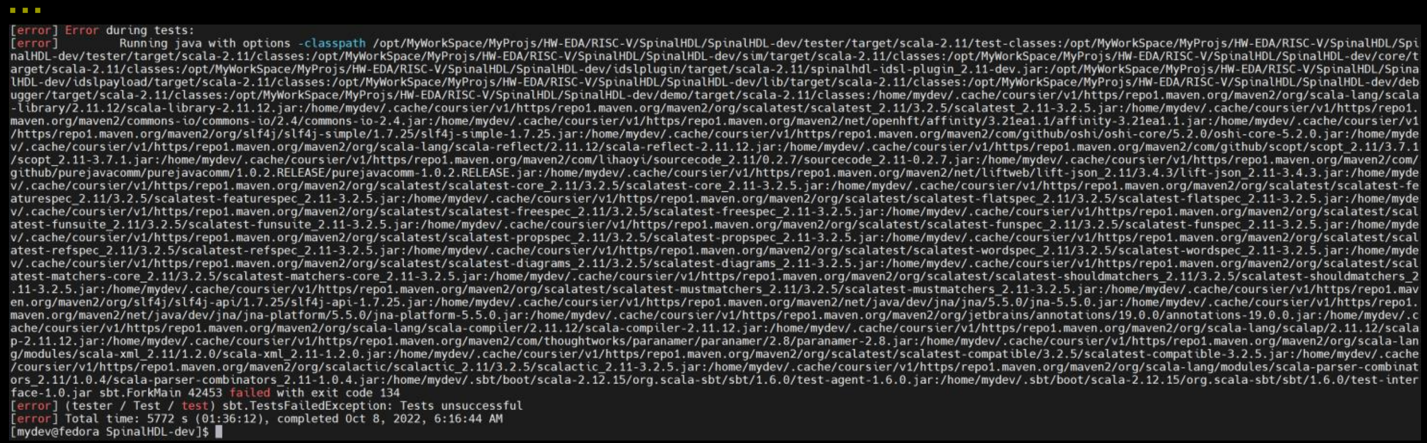
```
[mydev@fedora SpinalHDL-dev]$ git diff
diff --git a/build.sbt b/build.sbt
index b275d8cac..3086f45c4 100644
--- a/build.sbt
+++ b/build.sbt
@@ -14,13 +14,13 @@ val defaultSettings = Defaults.coreDefaultSettings ++ xerial.sbt.Sonatype.sonaty
   fork := true,

   //Enable parallel tests
-  Test / testForkedParallel := true,
-  testGrouping in Test := (testGrouping in Test).value.flatMap { group =>
+  Test / testForkedParallel := false,
+//  testGrouping in Test := (testGrouping in Test).value.flatMap { group =>
 //    for(i <- 0 until 4) yield {
 //      Group("g" + i,  group.tests.zipWithIndex.filter(_._2 % 4 == i).map(_._1), SubProcess(ForkOptions()))
 //    }
-    Seq(Group("g",  group.tests, SubProcess(ForkOptions())))
-  },
+//    Seq(Group("g",  group.tests, SubProcess(ForkOptions())))
+//  },
 //  concurrentRestrictions := Seq(Tags.limit(Tags.ForkedTestGroup, 4)),

   libraryDependencies += "org.scala-lang" % "scala-library" % scalaVersion.value,
[mydev@fedora SpinalHDL-dev]$
```



```
[mydev@fedora SpinalHDL-dev]$ sbt test
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/build.sbt:13: warning: method in in trait ScopingSetting is deprecated (since 1.5.0): `in` is deprecated; migrate to slash syntax - https://www
.scala-sbt.org/1.x/docs/Migrating-from-sbt-013x.html#slash
  baseDirectory in test := file("/out/"),
                ^
```

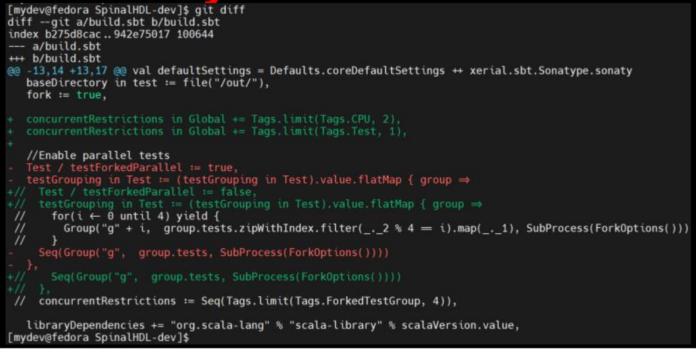


```
...
[Info] Test 'test' was reallocated as 'test_9' to avoid collision
[Progress] Start SpinalSimVerilatorIoTestTop test_9 simulation with seed 218567579
#
# If you would like to submit a bug report, please visit:
#   https://github.com/oracle/graal/issues
# The crash happened outside the Java Virtual Machine in native code.
# See problematic frame for where to report the bug.
#
- /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tmp/job_201/unamed.v:23: Verilog $finish
Exception in thread "Thread-8" java.io.EOFException
  | ⇒ tat java.base/java.io.ObjectInputStream$BlockDataInputStream.peekByte(ObjectInputStream.java:3239)
        at java.base/java.io.ObjectInputStream.readObject0(ObjectInputStream.java:1711)
        at java.base/java.io.ObjectInputStream.readObject(ObjectInputStream.java:538)
        at java.base/java.io.ObjectInputStream.readObject(ObjectInputStream.java:496)
        at org.scalatest.tools.Framework$ScalaTestRunner$Skeleton$1$React.react(Framework.scala:839)
        at org.scalatest.tools.Framework$ScalaTestRunner$Skeleton$1.run(Framework.scala:828)
        at java.base/java.lang.Thread.run(Thread.java:1589)
[info] Run completed in 1 hour, 31 minutes, 54 seconds.
[info] Total number of tests run: 478
[info] Suites: completed 48, aborted 0
[info] Tests: succeeded 470, failed 8, canceled 0, ignored 0, pending 0
[info] *** 8 TESTS FAILED ***
```

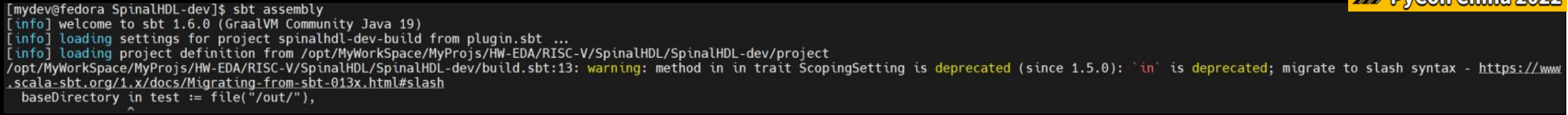


```
...
[error] Error during tests:
[error]         Running java with options -classpath /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/target/scala-2.11/test-classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/Spi
nalHDL-dev/tester/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/sim/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/core/t
arget/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslplugin/target/scala-2.11/spinalhdl-idsl-plugin_2.11-dev.jar:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/Spina
lHDL-dev/idslpayload/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/deb
ugger/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/demo/target/scala-2.11/classes:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scala
-library/2.11.12/scala-library-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest_2.11/3.2.5/scalatest_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.
maven.org/maven2/commons-io/commons-io/2.4/commons-io-2.4.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/net/openhft/affinity/3.21ea1.1/affinity-3.21ea1.1.jar:/home/mydev/.cache/coursier/v1
/https/repo1.maven.org/maven2/org/slf4j/slf4j-simple/1.7.25/slf4j-simple-1.7.25.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/github/oshi/oshi-core/5.2.0/oshi-core-5.2.0.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scala-reflect/2.11.12/scala-reflect-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/github/scopt/scopt_2.11/3.7.1
/scopt_2.11-3.7.1.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/lihaoyi/sourcecode_2.11/0.2.7/sourcecode_2.11-0.2.7.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/
github/purejavacomm/purejavacomm/1.0.2.RELEASE/purejavacomm-1.0.2.RELEASE.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/net/liftweb/lift-json_2.11/3.4.3/lift-json_2.11-3.4.3.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-core_2.11/3.2.5/scalatest-core_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-fe
aturespec_2.11/3.2.5/scalatest-featurespec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-flatspec_2.11/3.2.5/scalatest-flatspec_2.11-3.2.5.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-freespec_2.11/3.2.5/scalatest-freespec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scal
atest-funsuite_2.11/3.2.5/scalatest-funsuite_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-funspec_2.11/3.2.5/scalatest-funspec_2.11-3.2.5.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-propspec_2.11/3.2.5/scalatest-propspec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scal
atest-refspec_2.11/3.2.5/scalatest-refspec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-wordspec_2.11/3.2.5/scalatest-wordspec_2.11-3.2.5.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-diagrams_2.11/3.2.5/scalatest-diagrams_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scal
atest-matchers-core_2.11/3.2.5/scalatest-matchers-core_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-shouldmatchers_2.11/3.2.5/scalatest-shouldmatchers_2
.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-mustmatchers_2.11/3.2.5/scalatest-mustmatchers_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.mav
en.org/maven2/org/slf4j/slf4j-api/1.7.25/slf4j-api-1.7.25.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/net/java/dev/jna/jna/5.5.0/jna-5.5.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.
maven.org/maven2/net/java/dev/jna/jna-platform/5.5.0/jna-platform-5.5.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/jetbrains/annotations/19.0.0/annotations-19.0.0.jar:/home/mydev/.c
ache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scala-compiler/2.11.12/scala-compiler-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scalap/2.11.12/scala
p-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/thoughtworks/paranamer/paranamer/2.8/paranamer-2.8.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lan
g/modules/scala-xml_2.11/1.2.0/scala-xml_2.11-1.2.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-compatible/3.2.5/scalatest-compatible-3.2.5.jar:/home/mydev/.cache
/coursier/v1/https/repo1.maven.org/maven2/org/scalactic/scalactic_2.11/3.2.5/scalactic_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/modules/scala-parser-combinat
ors_2.11/1.0.4/scala-parser-combinators_2.11-1.0.4.jar:/home/mydev/.sbt/boot/scala-2.12.15/org.scala-sbt/sbt/1.6.0/test-agent-1.6.0.jar:/home/mydev/.sbt/boot/scala-2.12.15/org.scala-sbt/sbt/1.6.0/test-inter
face-1.0.jar sbt.ForkMain 42453 failed with exit code 134
[error] (tester / Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 5772 s (01:36:12), completed Oct 8, 2022, 6:16:44 AM
[mydev@fedora SpinalHDL-dev]$ █
```

- **Assembly**

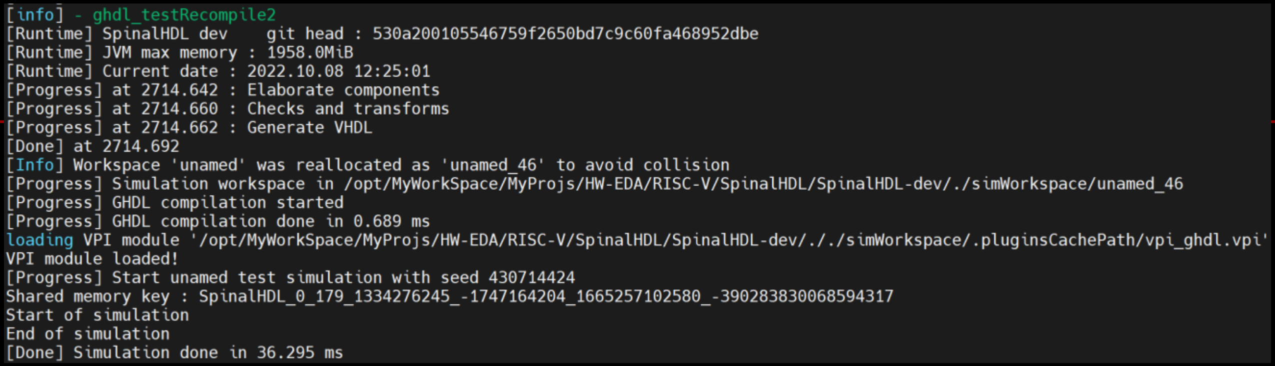


```
[mydev@fedora SpinalHDL-dev]$ git diff
diff --git a/build.sbt b/build.sbt
index b275d8cac..942e75017 100644
--- a/build.sbt
+++ b/build.sbt
@@ -13,14 +13,17 @@ val defaultSettings = Defaults.coreDefaultSettings ++ xerial.sbt.Sonatype.sonaty
   baseDirectory in test := file("/out/"),
   fork := true,

+  concurrentRestrictions in Global += Tags.limit(Tags.CPU, 2),
+  concurrentRestrictions in Global += Tags.limit(Tags.Test, 1),
+
   //Enable parallel tests
-  Test / testForkedParallel := true,
-  testGrouping in Test := (testGrouping in Test).value.flatMap { group ⇒
+//  Test / testForkedParallel := false,
+//  testGrouping in Test := (testGrouping in Test).value.flatMap { group ⇒
 //    for(i ← 0 until 4) yield {
 //      Group("g" + i,  group.tests.zipWithIndex.filter(_._2 % 4 == i).map(_._1), SubProcess(ForkOptions()))
 //    }
-    Seq(Group("g",  group.tests, SubProcess(ForkOptions())))
-  },
+//    Seq(Group("g",  group.tests, SubProcess(ForkOptions())))
+//  },
 //  concurrentRestrictions := Seq(Tags.limit(Tags.ForkedTestGroup, 4)),

   libraryDependencies += "org.scala-lang" % "scala-library" % scalaVersion.value,
[mydev@fedora SpinalHDL-dev]$
```



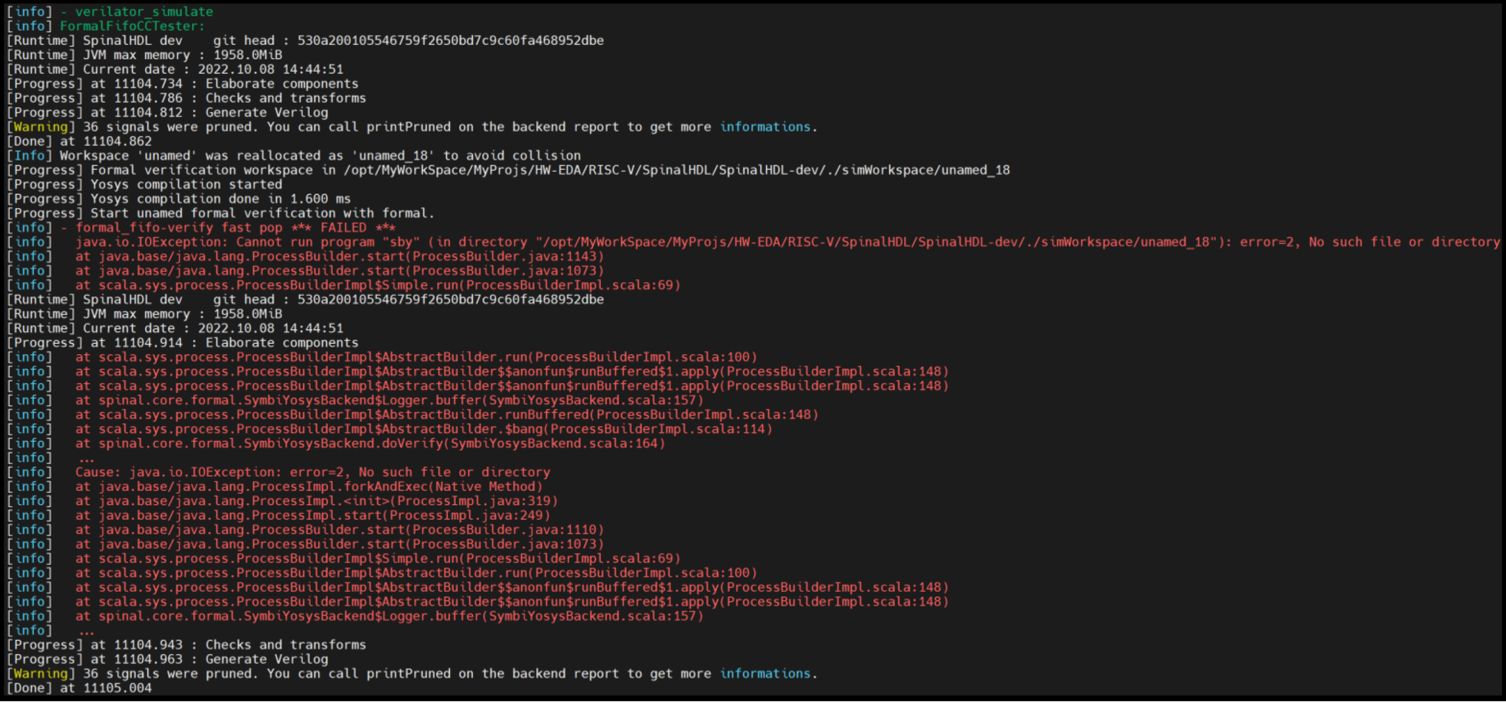
```
[mydev@fedora SpinalHDL-dev]$ sbt assembly
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/build.sbt:13: warning: method in in trait ScopingSetting is deprecated (since 1.5.0): `in` is deprecated; migrate to slash syntax - https://www
.scala-sbt.org/1.x/docs/Migrating-from-sbt-013x.html#slash
  baseDirectory in test := file("/out/"),
                ^
```

...



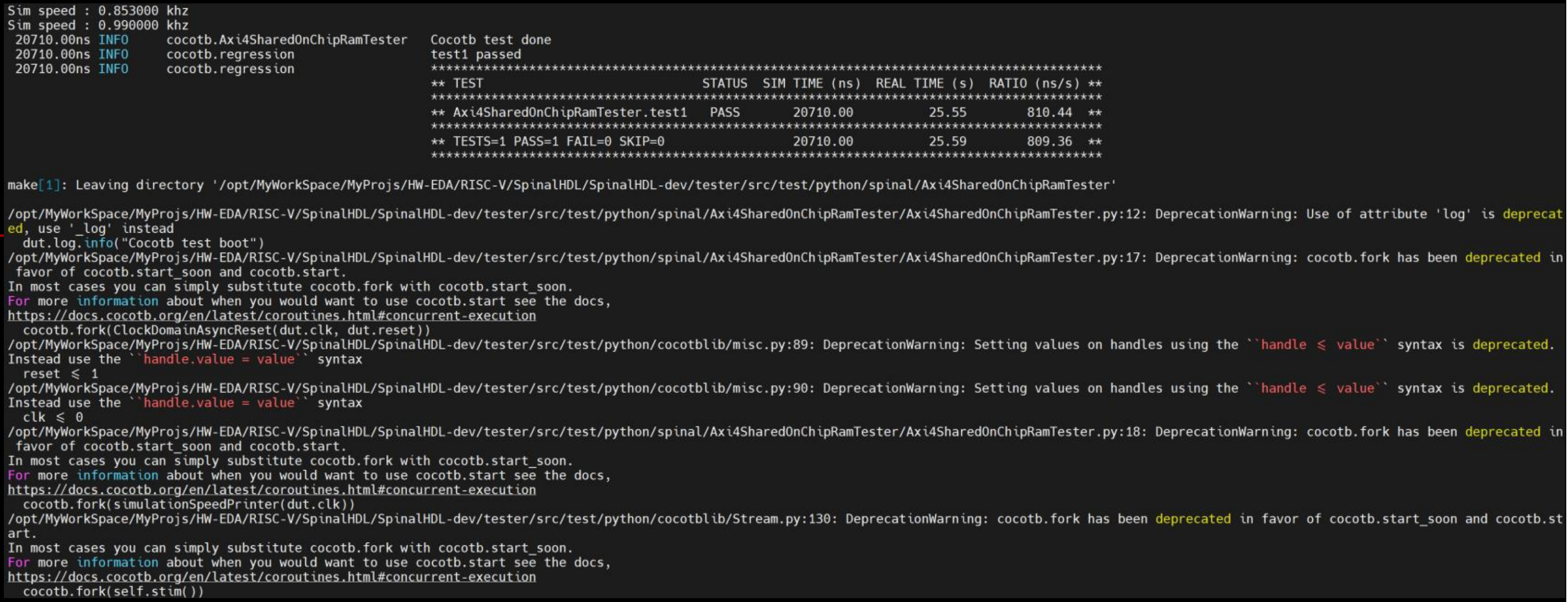
```
[info] - ghdl_testRecompile2
[Runtime] SpinalHDL dev    git head : 530a200105546759f2650bd7c9c60fa468952dbe
[Runtime] JVM max memory : 1958.0MiB
[Runtime] Current date : 2022.10.08 12:25:01
[Progress] at 2714.642 : Elaborate components
[Progress] at 2714.660 : Checks and transforms
[Progress] at 2714.662 : Generate VHDL
[Done] at 2714.692
[Info] Workspace 'unamed' was reallocated as 'unamed_46' to avoid collision
[Progress] Simulation workspace in /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/unamed_46
[Progress] GHDL compilation started
[Progress] GHDL compilation done in 0.689 ms
loading VPI module '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/././simWorkspace/.pluginsCachePath/vpi_ghdl.vpi'
VPI module loaded!
[Progress] Start unamed test simulation with seed 430714424
Shared memory key : SpinalHDL_0_179_1334276245_-1747164204_1665257102580_-390283830068594317
Start of simulation
End of simulation
[Done] Simulation done in 36.295 ms
```

...



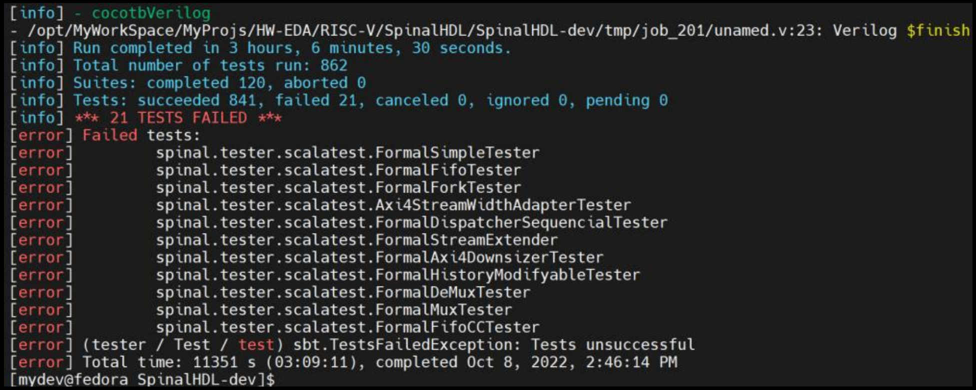
```
[info] - verilator_simulate
[info] FormalFifoCCTester:
[Runtime] SpinalHDL dev    git head : 530a200105546759f2650bd7c9c60fa468952dbe
[Runtime] JVM max memory : 1958.0MiB
[Runtime] Current date : 2022.10.08 14:44:51
[Progress] at 11104.734 : Elaborate components
[Progress] at 11104.786 : Checks and transforms
[Progress] at 11104.812 : Generate Verilog
[Warning] 36 signals were pruned. You can call printPruned on the backend report to get more informations.
[Done] at 11104.862
[Info] Workspace 'unamed' was reallocated as 'unamed_18' to avoid collision
[Progress] Formal verification workspace in /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/unamed_18
[Progress] Yosys compilation started
[Progress] Yosys compilation done in 1.600 ms
[Progress] Start unamed formal verification with formal.
[info] - formal_fifo-verify fast pop *** FAILED ***
[info]   java.io.IOException: Cannot run program "sby" (in directory "/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/unamed_18"): error=2, No such file or directory
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1143)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:69)
[Runtime] SpinalHDL dev    git head : 530a200105546759f2650bd7c9c60fa468952dbe
[Runtime] JVM max memory : 1958.0MiB
[Runtime] Current date : 2022.10.08 14:44:51
[Progress] at 11104.914 : Elaborate components
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:100)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at spinal.core.formal.SymbiYosysBackend$Logger.buffer(SymbiYosysBackend.scala:157)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.runBuffered(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.$bang(ProcessBuilderImpl.scala:114)
[info]   at spinal.core.formal.SymbiYosysBackend.doVerify(SymbiYosysBackend.scala:164)
[info]   ...
[info]   Cause: java.io.IOException: error=2, No such file or directory
[info]   at java.base/java.lang.ProcessImpl.forkAndExec(Native Method)
[info]   at java.base/java.lang.ProcessImpl.<init>(ProcessImpl.java:319)
[info]   at java.base/java.lang.ProcessImpl.start(ProcessImpl.java:249)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1110)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:69)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:100)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at spinal.core.formal.SymbiYosysBackend$Logger.buffer(SymbiYosysBackend.scala:157)
[info]   ...
[Progress] at 11104.943 : Checks and transforms
[Progress] at 11104.963 : Generate Verilog
[Warning] 36 signals were pruned. You can call printPruned on the backend report to get more informations.
[Done] at 11105.004
```

...



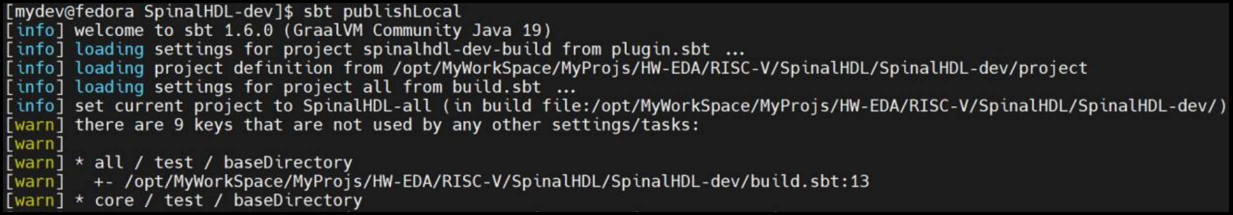
```
Sim speed : 0.853000 khz
Sim speed : 0.990000 khz
 20710.00ns INFO     cocotb.Axi4SharedOnChipRamTester   Cocotb test done
 20710.00ns INFO     cocotb.regression                  test1 passed
 20710.00ns INFO     cocotb.regression                  ******************************************************************************************
                                                        ** TEST                              STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                        ******************************************************************************************
                                                        ** Axi4SharedOnChipRamTester.test1   PASS       20710.00          25.55        810.44  **
                                                        ******************************************************************************************
                                                        ** TESTS=1 PASS=1 FAIL=0 SKIP=0                 20710.00          25.59        809.36  **
                                                        ******************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester'

/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester/Axi4SharedOnChipRamTester.py:12: DeprecationWarning: Use of attribute 'log' is deprecat
ed, use '_log' instead
  dut.log.info("Cocotb test boot")
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester/Axi4SharedOnChipRamTester.py:17: DeprecationWarning: cocotb.fork has been deprecated in
 favor of cocotb.start_soon and cocotb.start.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(ClockDomainAsyncReset(dut.clk, dut.reset))
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/misc.py:89: DeprecationWarning: Setting values on handles using the ``handle ≤ value`` syntax is deprecated.
Instead use the ``handle.value = value`` syntax
  reset ≤ 1
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/misc.py:90: DeprecationWarning: Setting values on handles using the ``handle ≤ value`` syntax is deprecated.
Instead use the ``handle.value = value`` syntax
  clk ≤ 0
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester/Axi4SharedOnChipRamTester.py:18: DeprecationWarning: cocotb.fork has been deprecated in
 favor of cocotb.start_soon and cocotb.start.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(simulationSpeedPrinter(dut.clk))
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/Stream.py:130: DeprecationWarning: cocotb.fork has been deprecated in favor of cocotb.start_soon and cocotb.st
art.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(self.stim())
```

...



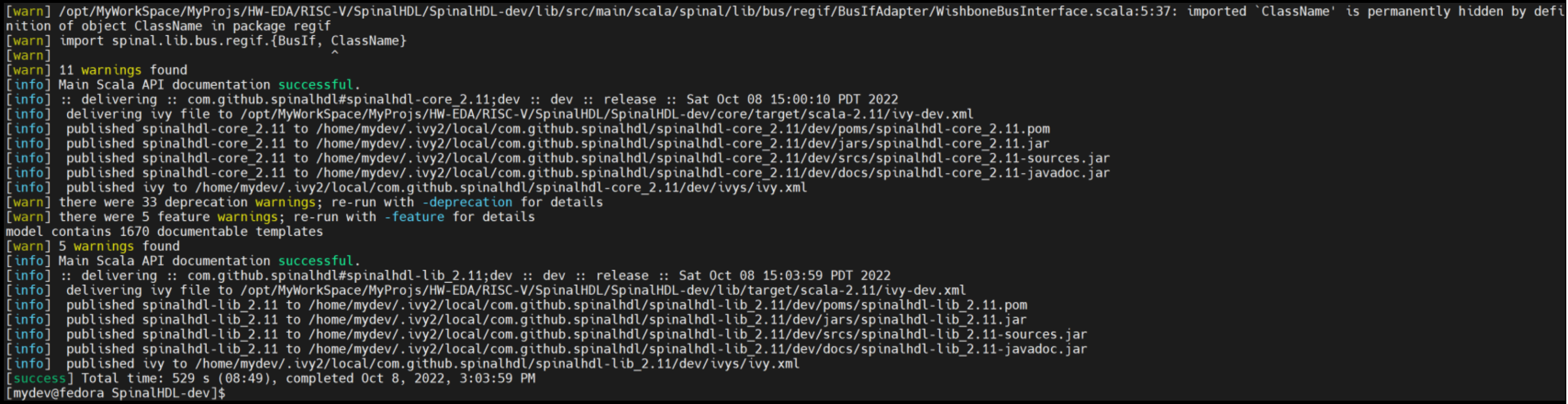
```
[info] - cocotbVerilog
- /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tmp/job_201/unamed.v:23: Verilog $finish
[info] Run completed in 3 hours, 6 minutes, 30 seconds.
[info] Total number of tests run: 862
[info] Suites: completed 120, aborted 0
[info] Tests: succeeded 841, failed 21, canceled 0, ignored 0, pending 0
[info] *** 21 TESTS FAILED ***
[error] Failed tests:
[error]         spinal.tester.scalatest.FormalSimpleTester
[error]         spinal.tester.scalatest.FormalFifoTester
[error]         spinal.tester.scalatest.FormalForkTester
[error]         spinal.tester.scalatest.Axi4StreamWidthAdapterTester
[error]         spinal.tester.scalatest.FormalDispatcherSequencialTester
[error]         spinal.tester.scalatest.FormalStreamExtender
[error]         spinal.tester.scalatest.FormalAxi4DownsizerTester
[error]         spinal.tester.scalatest.FormalHistoryModifyableTester
[error]         spinal.tester.scalatest.FormalDeMuxTester
[error]         spinal.tester.scalatest.FormalMuxTester
[error]         spinal.tester.scalatest.FormalFifoCCTester
[error] (tester / Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 11351 s (03:09:11), completed Oct 8, 2022, 2:46:14 PM
[mydev@fedora SpinalHDL-dev]$
```

Publish

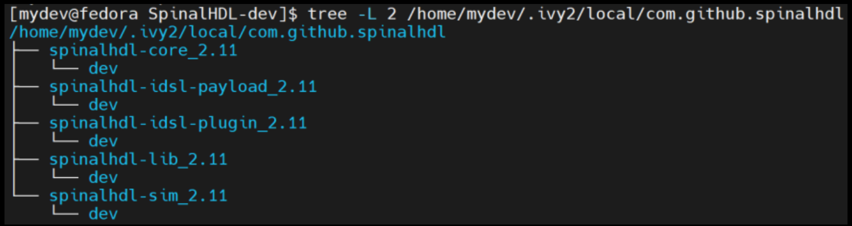


```
[mydev@fedora SpinalHDL-dev]$ sbt publishLocal
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] loading settings for project all from build.sbt ...
[info] set current project to SpinalHDL-all (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/)
[warn] there are 9 keys that are not used by any other settings/tasks:
[warn]
[warn] * all / test / baseDirectory
[warn]   +- /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/build.sbt:13
[warn] * core / test / baseDirectory
```

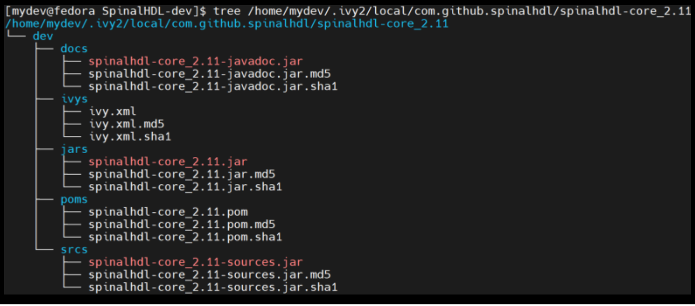
...



```
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/src/main/scala/spinal/lib/bus/regif/BusIfAdapter/WishboneBusInterface.scala:5:37: imported `ClassName' is permanently hidden by defi
nition of object ClassName in package regif
[warn] import spinal.lib.bus.regif.{BusIf, ClassName}
[warn]                                      ^
[warn] 11 warnings found
[info] Main Scala API documentation successful.
[info] :: delivering :: com.github.spinalhdl#spinalhdl-core_2.11;dev :: dev :: release :: Sat Oct 08 15:00:10 PDT 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/core/target/scala-2.11/ivy-dev.xml
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/poms/spinalhdl-core_2.11.pom
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/jars/spinalhdl-core_2.11.jar
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/srcs/spinalhdl-core_2.11-sources.jar
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/docs/spinalhdl-core_2.11-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/ivys/ivy.xml
[warn] there were 33 deprecation warnings; re-run with -deprecation for details
[warn] there were 5 feature warnings; re-run with -feature for details
model contains 1670 documentable templates
[warn] 5 warnings found
[info] Main Scala API documentation successful.
[info] :: delivering :: com.github.spinalhdl#spinalhdl-lib_2.11;dev :: dev :: release :: Sat Oct 08 15:03:59 PDT 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/target/scala-2.11/ivy-dev.xml
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/poms/spinalhdl-lib_2.11.pom
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/jars/spinalhdl-lib_2.11.jar
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/srcs/spinalhdl-lib_2.11-sources.jar
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/docs/spinalhdl-lib_2.11-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/ivys/ivy.xml
[success] Total time: 529 s (08:49), completed Oct 8, 2022, 3:03:59 PM
[mydev@fedora SpinalHDL-dev]$
```



```
[mydev@fedora SpinalHDL-dev]$ tree -L 2 /home/mydev/.ivy2/local/com.github.spinalhdl
/home/mydev/.ivy2/local/com.github.spinalhdl
├── spinalhdl-core_2.11
│   └── dev
├── spinalhdl-idsl-payload_2.11
│   └── dev
├── spinalhdl-idsl-plugin_2.11
│   └── dev
├── spinalhdl-lib_2.11
│   └── dev
└── spinalhdl-sim_2.11
    └── dev
```



```
[mydev@fedora SpinalHDL-dev]$ tree /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11
/home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11
└── dev
    ├── docs
    │   ├── spinalhdl-core_2.11-javadoc.jar
    │   ├── spinalhdl-core_2.11-javadoc.jar.md5
    │   └── spinalhdl-core_2.11-javadoc.jar.sha1
    ├── ivys
    │   ├── ivy.xml
    │   ├── ivy.xml.md5
    │   └── ivy.xml.sha1
    ├── jars
    │   ├── spinalhdl-core_2.11.jar
    │   ├── spinalhdl-core_2.11.jar.md5
    │   └── spinalhdl-core_2.11.jar.sha1
    ├── poms
    │   ├── spinalhdl-core_2.11.pom
    │   ├── spinalhdl-core_2.11.pom.md5
    │   └── spinalhdl-core_2.11.pom.sha1
    └── srcs
        ├── spinalhdl-core_2.11-sources.jar
        ├── spinalhdl-core_2.11-sources.jar.md5
        └── spinalhdl-core_2.11-sources.jar.sha1
```

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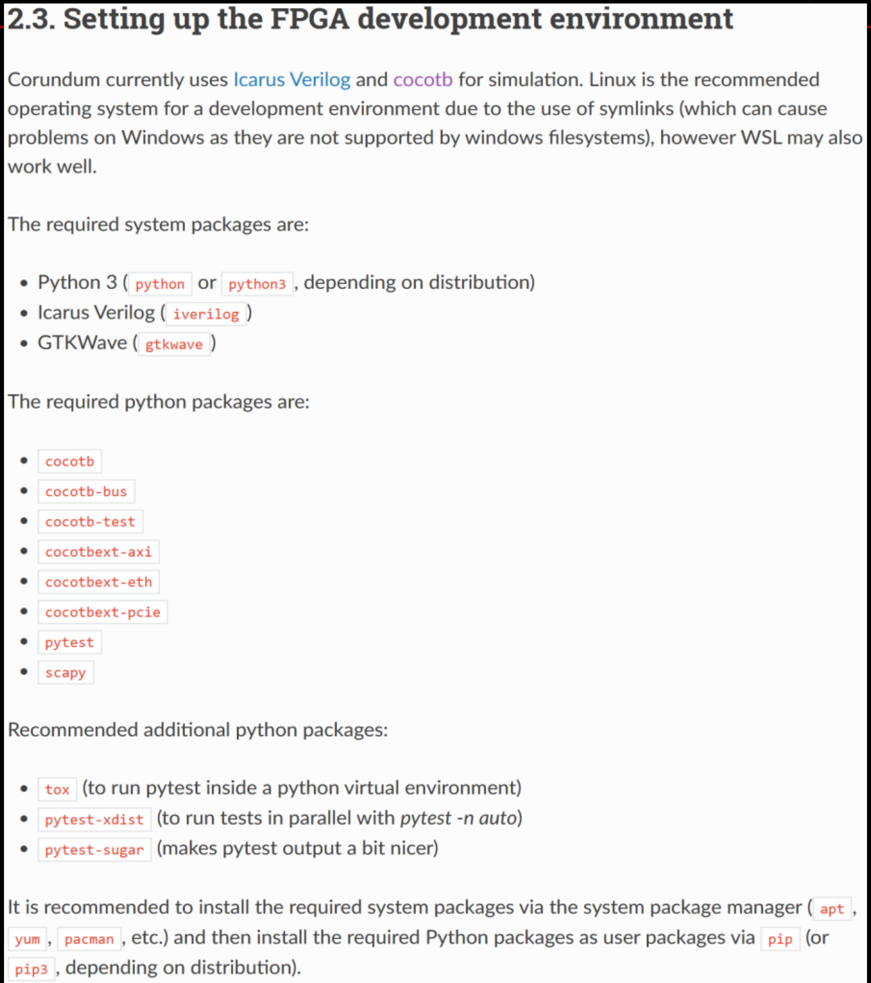
III. Corundum with Cocotb on ARM

Prerequisites

- https://docs.corundum.io/en/latest/gettingstarted.html



2.3. Setting up the FPGA development environment

Corundum currently uses Icarus Verilog and cocotb for simulation. Linux is the recommended operating system for a development environment due to the use of symlinks (which can cause problems on Windows as they are not supported by windows filesystems), however WSL may also work well.

The required system packages are:

- Python 3 (`python` or `python3` , depending on distribution)
- Icarus Verilog (`iverilog`)
- GTKWave (`gtkwave`)

The required python packages are:

- `cocotb`
- `cocotb-bus`
- `cocotb-test`
- `cocotbext-axi`
- `cocotbext-eth`
- `cocotbext-pcie`
- `pytest`
- `scapy`

Recommended additional python packages:

- `tox` (to run pytest inside a python virtual environment)
- `pytest-xdist` (to run tests in parallel with *pytest -n auto*)
- `pytest-sugar` (makes pytest output a bit nicer)

It is recommended to install the required system packages via the system package manager (`apt` , `yum` , `pacman` , etc.) and then install the required Python packages as user packages via `pip` (or `pip3` , depending on distribution).

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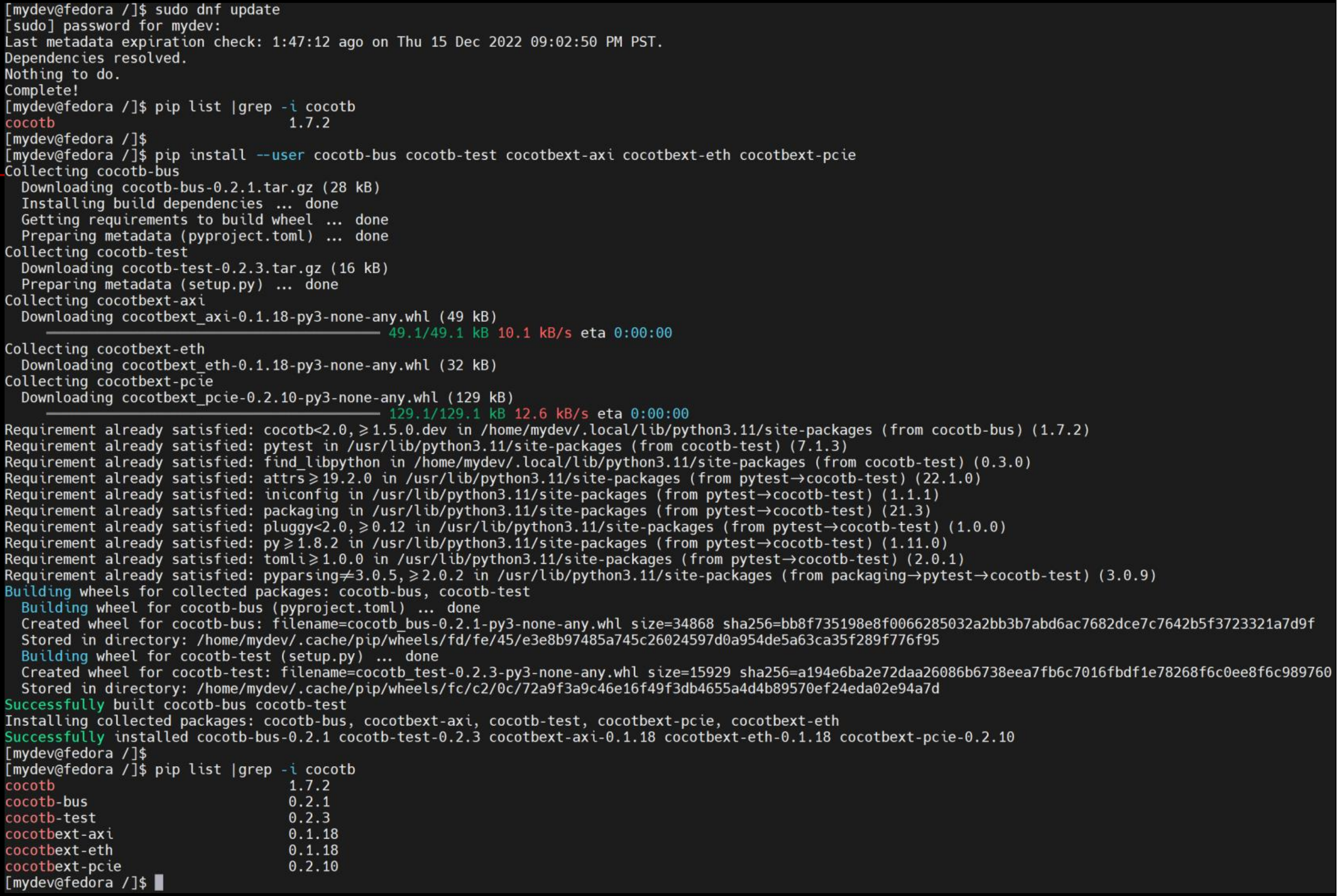
Setup

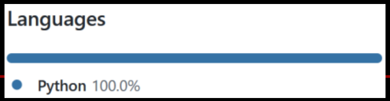


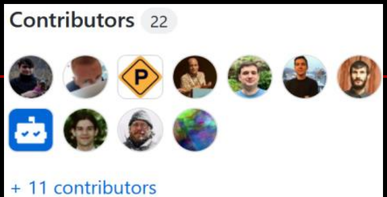
```
[mydev@fedora /]$ sudo dnf update
[sudo] password for mydev:
Last metadata expiration check: 1:47:12 ago on Thu 15 Dec 2022 09:02:50 PM PST.
Dependencies resolved.
Nothing to do.
Complete!
[mydev@fedora /]$ pip list |grep -i cocotb
cocotb                            1.7.2
[mydev@fedora /]$
[mydev@fedora /]$ pip install --user cocotb-bus cocotb-test cocotbext-axi cocotbext-eth cocotbext-pcie
Collecting cocotb-bus
  Downloading cocotb-bus-0.2.1.tar.gz (28 kB)
  Installing build dependencies ... done
  Getting requirements to build wheel ... done
  Preparing metadata (pyproject.toml) ... done
Collecting cocotb-test
  Downloading cocotb-test-0.2.3.tar.gz (16 kB)
  Preparing metadata (setup.py) ... done
Collecting cocotbext-axi
  Downloading cocotbext_axi-0.1.18-py3-none-any.whl (49 kB)
     ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 49.1/49.1 kB 10.1 kB/s eta 0:00:00
Collecting cocotbext-eth
  Downloading cocotbext_eth-0.1.18-py3-none-any.whl (32 kB)
Collecting cocotbext-pcie
  Downloading cocotbext_pcie-0.2.10-py3-none-any.whl (129 kB)
     ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 129.1/129.1 kB 12.6 kB/s eta 0:00:00
Requirement already satisfied: cocotb<2.0,≥1.5.0.dev in /home/mydev/.local/lib/python3.11/site-packages (from cocotb-bus) (1.7.2)
Requirement already satisfied: pytest in /usr/lib/python3.11/site-packages (from cocotb-test) (7.1.3)
Requirement already satisfied: find_libpython in /home/mydev/.local/lib/python3.11/site-packages (from cocotb-test) (0.3.0)
Requirement already satisfied: attrs≥19.2.0 in /usr/lib/python3.11/site-packages (from pytest→cocotb-test) (22.1.0)
Requirement already satisfied: iniconfig in /usr/lib/python3.11/site-packages (from pytest→cocotb-test) (1.1.1)
Requirement already satisfied: packaging in /usr/lib/python3.11/site-packages (from pytest→cocotb-test) (21.3)
Requirement already satisfied: pluggy<2.0,≥0.12 in /usr/lib/python3.11/site-packages (from pytest→cocotb-test) (1.0.0)
Requirement already satisfied: py≥1.8.2 in /usr/lib/python3.11/site-packages (from pytest→cocotb-test) (1.11.0)
Requirement already satisfied: tomli≥1.0.0 in /usr/lib/python3.11/site-packages (from pytest→cocotb-test) (2.0.1)
Requirement already satisfied: pyparsing≠3.0.5,≥2.0.2 in /usr/lib/python3.11/site-packages (from packaging→pytest→cocotb-test) (3.0.9)
Building wheels for collected packages: cocotb-bus, cocotb-test
  Building wheel for cocotb-bus (pyproject.toml) ... done
  Created wheel for cocotb-bus: filename=cocotb_bus-0.2.1-py3-none-any.whl size=34868 sha256=bb8f735198e8f0066285032a2bb3b7abd6ac7682dce7c7642b5f3723321a7d9f
  Stored in directory: /home/mydev/.cache/pip/wheels/fd/fe/45/e3e8b97485a745c26024597d0a954de5a63ca35f289f776f95
  Building wheel for cocotb-test (setup.py) ... done
  Created wheel for cocotb-test: filename=cocotb_test-0.2.3-py3-none-any.whl size=15929 sha256=a194e6ba2e72daa26086b6738eea7fb6c7016fbdf1e78268f6c0ee8f6c989760
  Stored in directory: /home/mydev/.cache/pip/wheels/fc/c2/0c/72a9f3a9c46e16f49f3db4655a4d4b89570ef24eda02e94a7d
Successfully built cocotb-bus cocotb-test
Installing collected packages: cocotb-bus, cocotbext-axi, cocotb-test, cocotbext-pcie, cocotbext-eth
Successfully installed cocotb-bus-0.2.1 cocotb-test-0.2.3 cocotbext-axi-0.1.18 cocotbext-eth-0.1.18 cocotbext-pcie-0.2.10
[mydev@fedora /]$
[mydev@fedora /]$ pip list |grep -i cocotb
cocotb                            1.7.2
cocotb-bus                        0.2.1
cocotb-test                       0.2.3
cocotbext-axi                     0.1.18
cocotbext-eth                     0.1.18
cocotbext-pcie                    0.2.10
[mydev@fedora /]$ █
```

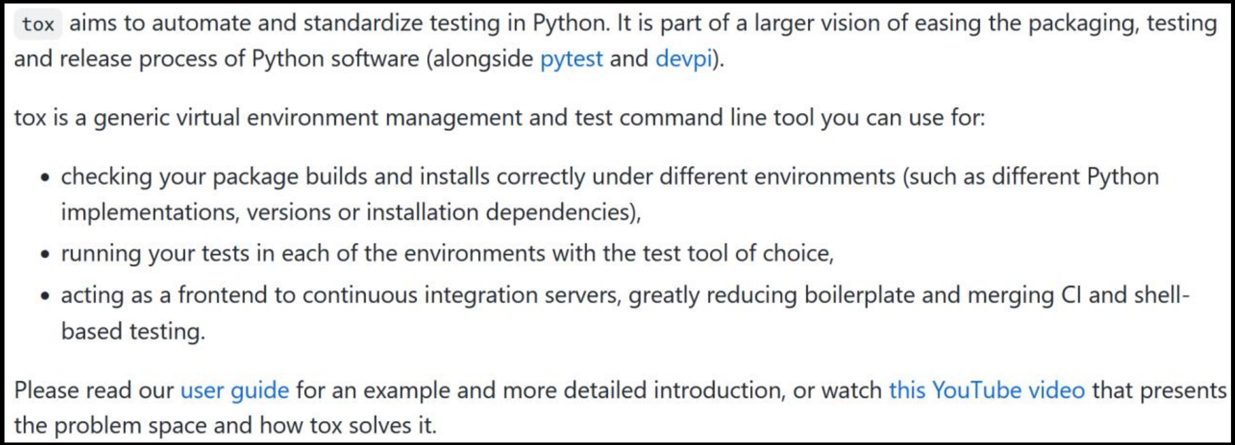
sudo dnf install python3-scapy python3-pytest-xdist python3-pytest-sugar…

- tox

https://tox.wiki/en/latest/
https://github.com/tox-dev/tox







`tox` aims to automate and standardize testing in Python. It is part of a larger vision of easing the packaging, testing and release process of Python software (alongside pytest and devpi).

tox is a generic virtual environment management and test command line tool you can use for:

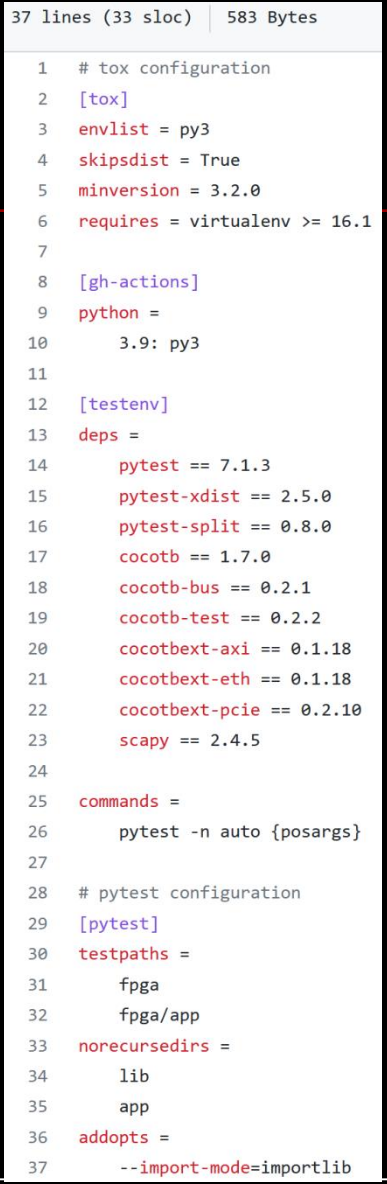
- checking your package builds and installs correctly under different environments (such as different Python implementations, versions or installation dependencies),
- running your tests in each of the environments with the test tool of choice,
- acting as a frontend to continuous integration servers, greatly reducing boilerplate and merging CI and shell-based testing.

Please read our user guide for an example and more detailed introduction, or watch this YouTube video that presents the problem space and how tox solves it.

https://wiki.openstack.org/wiki/Testing

…

https://github.com/corundum/corundum/blob/master/tox.ini



37 lines (33 sloc) | 583 Bytes

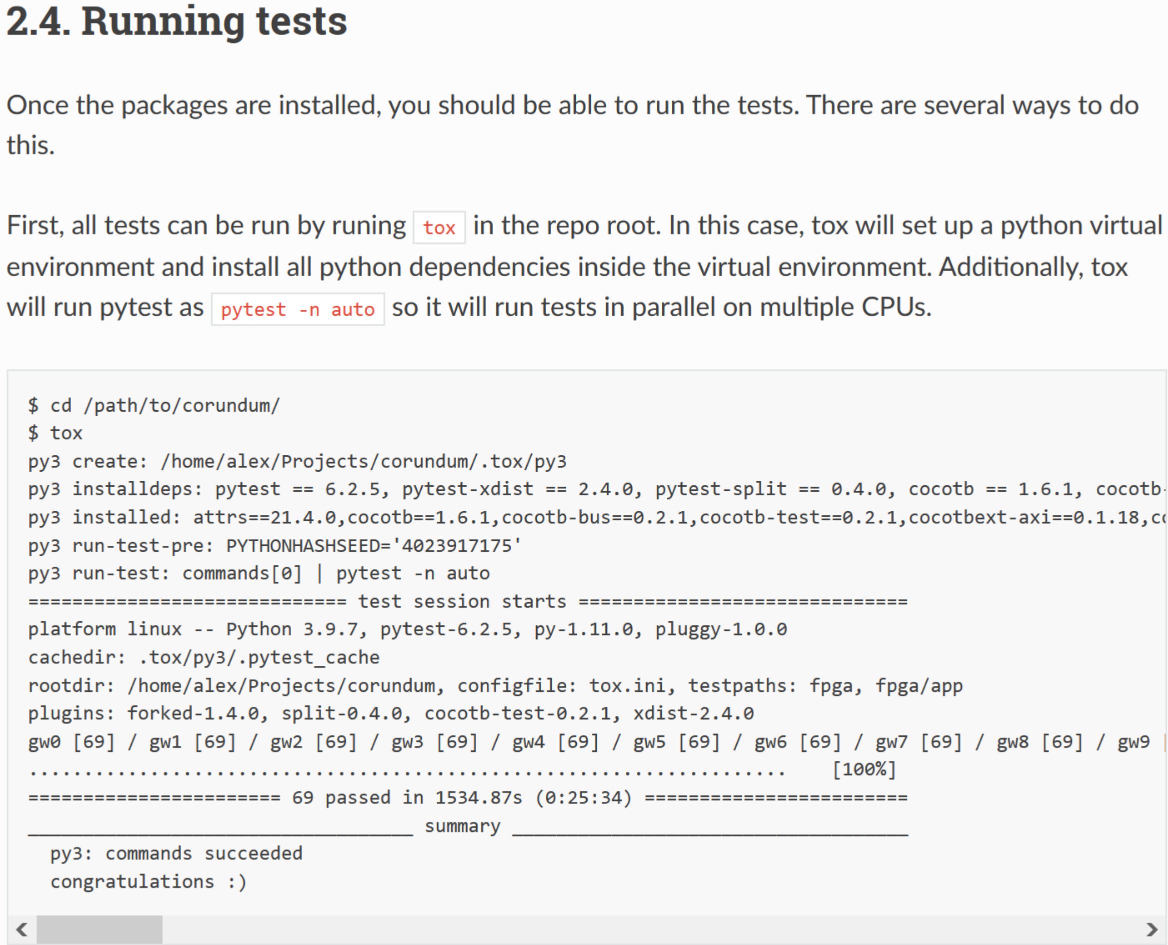
```ini
# tox configuration
[tox]
envlist = py3
skipsdist = True
minversion = 3.2.0
requires = virtualenv >= 16.1

[gh-actions]
python =
    3.9: py3

[testenv]
deps =
    pytest == 7.1.3
    pytest-xdist == 2.5.0
    pytest-split == 0.8.0
    cocotb == 1.7.0
    cocotb-bus == 0.2.1
    cocotb-test == 0.2.2
    cocotbext-axi == 0.1.18
    cocotbext-eth == 0.1.18
    cocotbext-pcie == 0.2.10
    scapy == 2.4.5

commands =
    pytest -n auto {posargs}

# pytest configuration
[pytest]
testpaths =
    fpga
    fpga/app
norecursedirs =
    lib
    app
addopts =
    --import-mode=importlib
```

1) RPi4

1.1 Running Tests

Official Guide

- https://docs.corundum.io/en/latest/gettingstarted.html

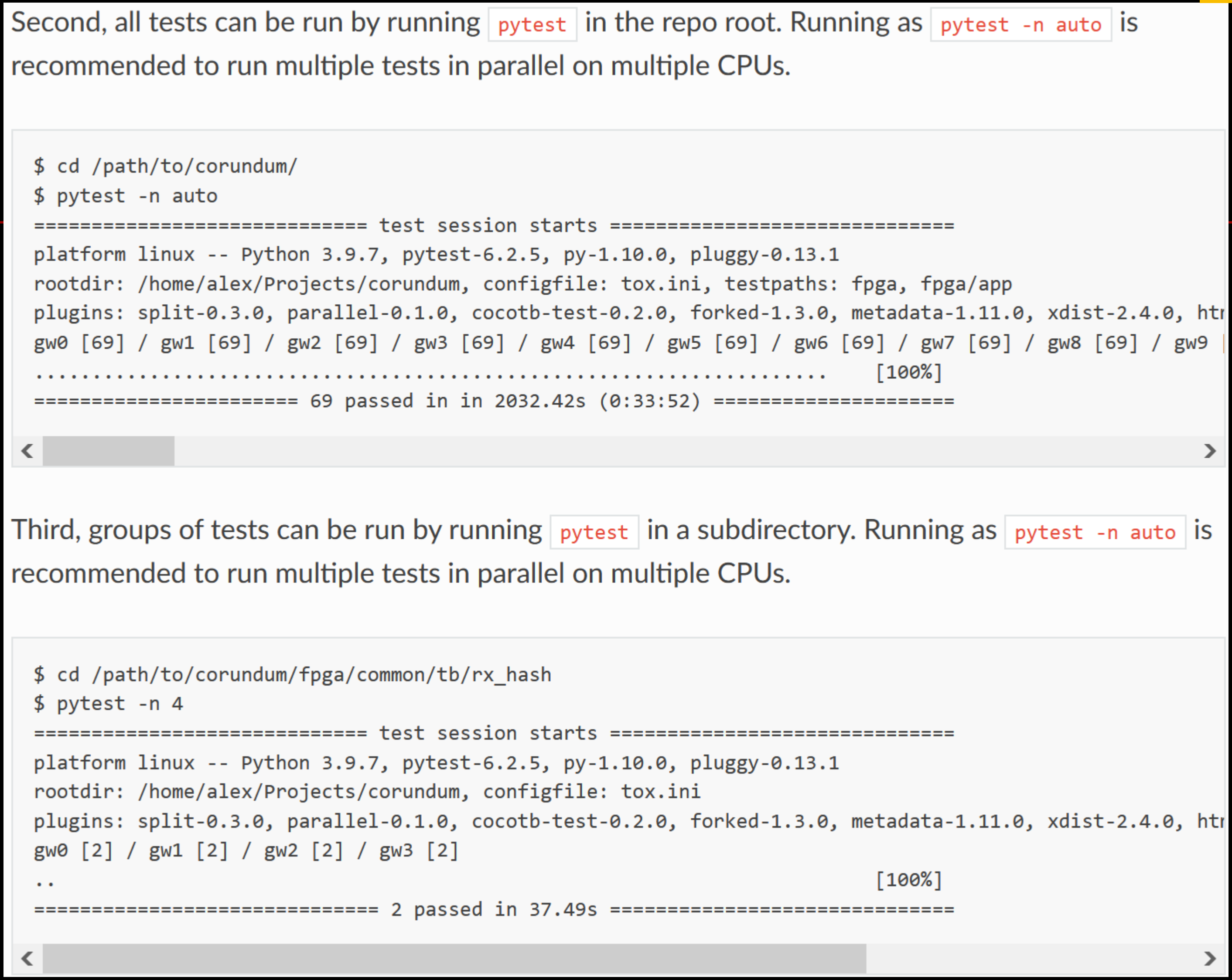


2.4. Running tests

Once the packages are installed, you should be able to run the tests. There are several ways to do this.

First, all tests can be run by runing `tox` in the repo root. In this case, tox will set up a python virtual environment and install all python dependencies inside the virtual environment. Additionally, tox will run pytest as `pytest -n auto` so it will run tests in parallel on multiple CPUs.

```
$ cd /path/to/corundum/
$ tox
py3 create: /home/alex/Projects/corundum/.tox/py3
py3 installdeps: pytest == 6.2.5, pytest-xdist == 2.4.0, pytest-split == 0.4.0, cocotb == 1.6.1, cocotb
py3 installed: attrs==21.4.0,cocotb==1.6.1,cocotb-bus==0.2.1,cocotb-test==0.2.1,cocotbext-axi==0.1.18,c
py3 run-test-pre: PYTHONHASHSEED='4023917175'
py3 run-test: commands[0] | pytest -n auto
============================= test session starts ==============================
platform linux -- Python 3.9.7, pytest-6.2.5, py-1.11.0, pluggy-1.0.0
cachedir: .tox/py3/.pytest_cache
rootdir: /home/alex/Projects/corundum, configfile: tox.ini, testpaths: fpga, fpga/app
plugins: forked-1.4.0, split-0.4.0, cocotb-test-0.2.1, xdist-2.4.0
gw0 [69] / gw1 [69] / gw2 [69] / gw3 [69] / gw4 [69] / gw5 [69] / gw6 [69] / gw7 [69] / gw8 [69] / gw9
.....................................................................    [100%]
======================= 69 passed in 1534.87s (0:25:34) ========================
___________________________________ summary ____________________________________
  py3: commands succeeded
  congratulations :)
```

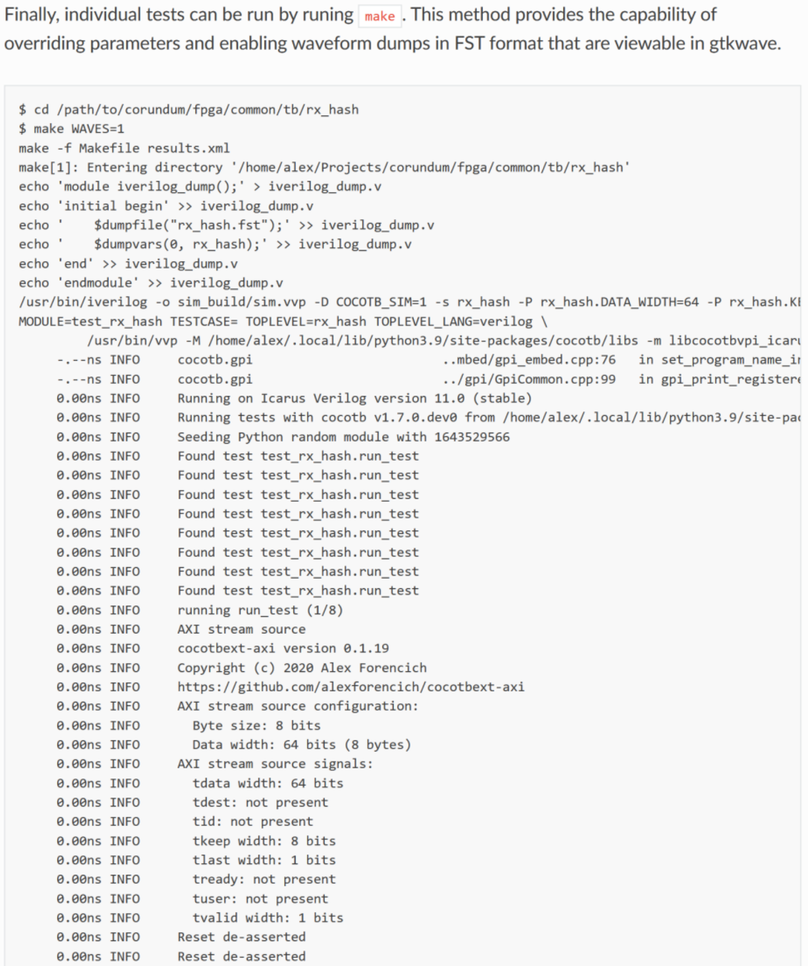


Second, all tests can be run by running `pytest` in the repo root. Running as `pytest -n auto` is recommended to run multiple tests in parallel on multiple CPUs.

```
$ cd /path/to/corundum/
$ pytest -n auto
============================= test session starts ==============================
platform linux -- Python 3.9.7, pytest-6.2.5, py-1.10.0, pluggy-0.13.1
rootdir: /home/alex/Projects/corundum, configfile: tox.ini, testpaths: fpga, fpga/app
plugins: split-0.3.0, parallel-0.1.0, cocotb-test-0.2.0, forked-1.3.0, metadata-1.11.0, xdist-2.4.0, ht
gw0 [69] / gw1 [69] / gw2 [69] / gw3 [69] / gw4 [69] / gw5 [69] / gw6 [69] / gw7 [69] / gw8 [69] / gw9
.....................................................................     [100%]
======================= 69 passed in in 2032.42s (0:33:52) =====================
```

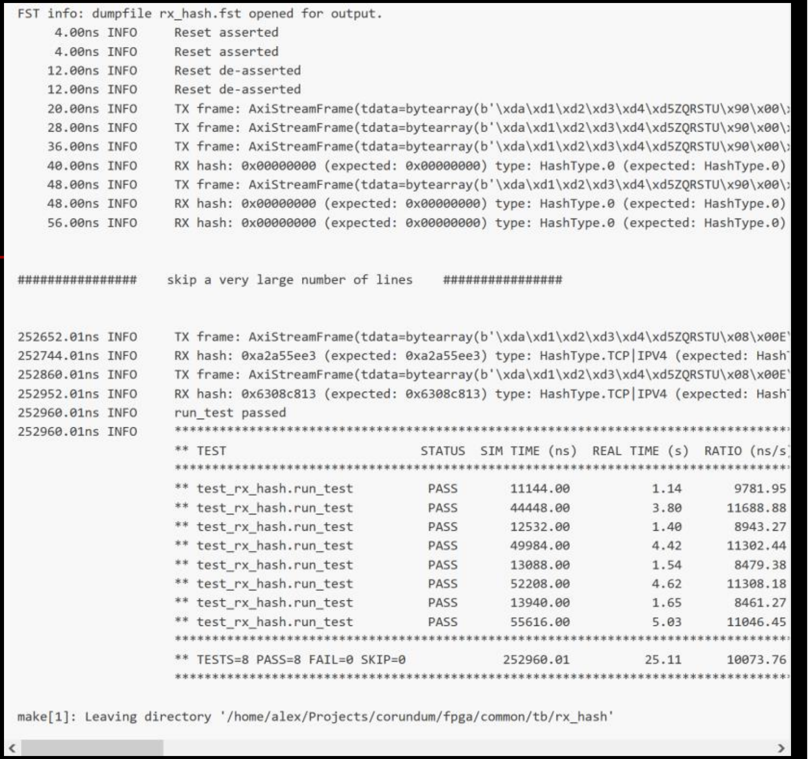
Third, groups of tests can be run by running `pytest` in a subdirectory. Running as `pytest -n auto` is recommended to run multiple tests in parallel on multiple CPUs.

```
$ cd /path/to/corundum/fpga/common/tb/rx_hash
$ pytest -n 4
============================= test session starts ==============================
platform linux -- Python 3.9.7, pytest-6.2.5, py-1.10.0, pluggy-0.13.1
rootdir: /home/alex/Projects/corundum, configfile: tox.ini
plugins: split-0.3.0, parallel-0.1.0, cocotb-test-0.2.0, forked-1.3.0, metadata-1.11.0, xdist-2.4.0, ht
gw0 [2] / gw1 [2] / gw2 [2] / gw3 [2]
..                                                                        [100%]
============================== 2 passed in 37.49s ==============================
```



Finally, individual tests can be run by runing `make`. This method provides the capability of overriding parameters and enabling waveform dumps in FST format that are viewable in gtkwave.

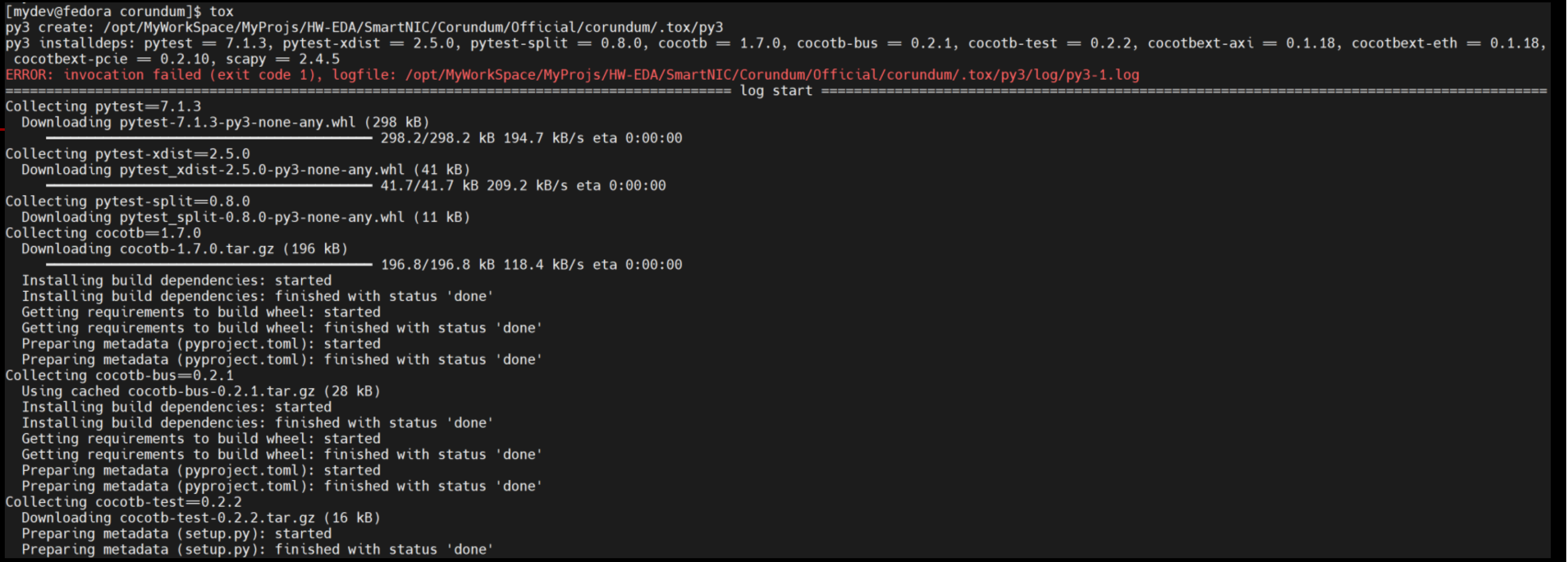
```
$ cd /path/to/corundum/fpga/common/tb/rx_hash
$ make WAVES=1
make -f Makefile results.xml
make[1]: Entering directory '/home/alex/Projects/corundum/fpga/common/tb/rx_hash'
echo 'module iverilog_dump();' > iverilog_dump.v
echo 'initial begin' >> iverilog_dump.v
echo '    $dumpfile("rx_hash.fst");' >> iverilog_dump.v
echo '    $dumpvars(0, rx_hash);' >> iverilog_dump.v
echo 'end' >> iverilog_dump.v
echo 'endmodule' >> iverilog_dump.v
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s rx_hash -P rx_hash.DATA_WIDTH=64 -P rx_hash.K
MODULE=test_rx_hash TESTCASE= TOPLEVEL=rx_hash TOPLEVEL_LANG=verilog \
         /usr/bin/vvp -M /home/alex/.local/lib/python3.9/site-packages/cocotb/libs -m libcocotbvpi_icaru
     -.--ns INFO     cocotb.gpi                         ..mbed/gpi_embed.cpp:76   in set_program_name_i
     -.--ns INFO     cocotb.gpi                         ../gpi/GpiCommon.cpp:99   in gpi_print_registere
     0.00ns INFO     Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     Running tests with cocotb v1.7.0.dev0 from /home/alex/.local/lib/python3.9/site-pa
     0.00ns INFO     Seeding Python random module with 1643529566
     0.00ns INFO     Found test test_rx_hash.run_test
     0.00ns INFO     Found test test_rx_hash.run_test
     0.00ns INFO     Found test test_rx_hash.run_test
     0.00ns INFO     Found test test_rx_hash.run_test
     0.00ns INFO     Found test test_rx_hash.run_test
     0.00ns INFO     Found test test_rx_hash.run_test
     0.00ns INFO     Found test test_rx_hash.run_test
     0.00ns INFO     Found test test_rx_hash.run_test
     0.00ns INFO     running run_test (1/8)
     0.00ns INFO     AXI stream source
     0.00ns INFO     cocotbext-axi version 0.1.19
     0.00ns INFO     Copyright (c) 2020 Alex Forencich
     0.00ns INFO     https://github.com/alexforencich/cocotbext-axi
     0.00ns INFO     AXI stream source configuration:
     0.00ns INFO       Byte size: 8 bits
     0.00ns INFO       Data width: 64 bits (8 bytes)
     0.00ns INFO     AXI stream source signals:
     0.00ns INFO       tdata width: 64 bits
     0.00ns INFO       tdest: not present
     0.00ns INFO       tid: not present
     0.00ns INFO       tkeep width: 8 bits
     0.00ns INFO       tlast width: 1 bits
     0.00ns INFO       tready: not present
     0.00ns INFO       tuser: not present
     0.00ns INFO       tvalid width: 1 bits
     0.00ns INFO     Reset de-asserted
     0.00ns INFO     Reset de-asserted
```



```
FST info: dumpfile rx_hash.fst opened for output.
     4.00ns INFO     Reset asserted
     4.00ns INFO     Reset asserted
    12.00ns INFO     Reset de-asserted
    12.00ns INFO     Reset de-asserted
    20.00ns INFO     TX frame: AxiStreamFrame(tdata=bytearray(b'\xda\xd1\xd2\xd3\xd4\xd5ZQRSTU\x90\x00\
    28.00ns INFO     TX frame: AxiStreamFrame(tdata=bytearray(b'\xda\xd1\xd2\xd3\xd4\xd5ZQRSTU\x90\x00\
    36.00ns INFO     TX frame: AxiStreamFrame(tdata=bytearray(b'\xda\xd1\xd2\xd3\xd4\xd5ZQRSTU\x90\x00\
    40.00ns INFO     RX hash: 0x00000000 (expected: 0x00000000) type: HashType.0 (expected: HashType.0)
    48.00ns INFO     TX frame: AxiStreamFrame(tdata=bytearray(b'\xda\xd1\xd2\xd3\xd4\xd5ZQRSTU\x90\x00\
    48.00ns INFO     RX hash: 0x00000000 (expected: 0x00000000) type: HashType.0 (expected: HashType.0)
    56.00ns INFO     RX hash: 0x00000000 (expected: 0x00000000) type: HashType.0 (expected: HashType.0)


################    skip a very large number of lines    ################


252652.01ns INFO     TX frame: AxiStreamFrame(tdata=bytearray(b'\xda\xd1\xd2\xd3\xd4\xd5ZQRSTU\x08\x00E
252744.01ns INFO     RX hash: 0xa2a55ee3 (expected: 0xa2a55ee3) type: HashType.TCP|IPV4 (expected: Hash
252860.01ns INFO     TX frame: AxiStreamFrame(tdata=bytearray(b'\xda\xd1\xd2\xd3\xd4\xd5ZQRSTU\x08\x00E
252952.01ns INFO     RX hash: 0x6308c813 (expected: 0x6308c813) type: HashType.TCP|IPV4 (expected: Hash
252960.01ns INFO     run_test passed
252960.01ns INFO     **************************************************************************************
                     ** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s
                     **************************************************************************************
                     ** test_rx_hash.run_test          PASS        11144.00           1.14        9781.95
                     ** test_rx_hash.run_test          PASS        44448.00           3.80       11688.88
                     ** test_rx_hash.run_test          PASS        12532.00           1.40        8943.27
                     ** test_rx_hash.run_test          PASS        49984.00           4.42       11302.44
                     ** test_rx_hash.run_test          PASS        13088.00           1.54        8479.38
                     ** test_rx_hash.run_test          PASS        52208.00           4.62       11308.18
                     ** test_rx_hash.run_test          PASS        13940.00           1.65        8461.27
                     ** test_rx_hash.run_test          PASS        55616.00           5.03       11046.45
                     **************************************************************************************
                     ** TESTS=8 PASS=8 FAIL=0 SKIP=0              252960.01          25.11       10073.76
                     **************************************************************************************

make[1]: Leaving directory '/home/alex/Projects/corundum/fpga/common/tb/rx_hash'
```

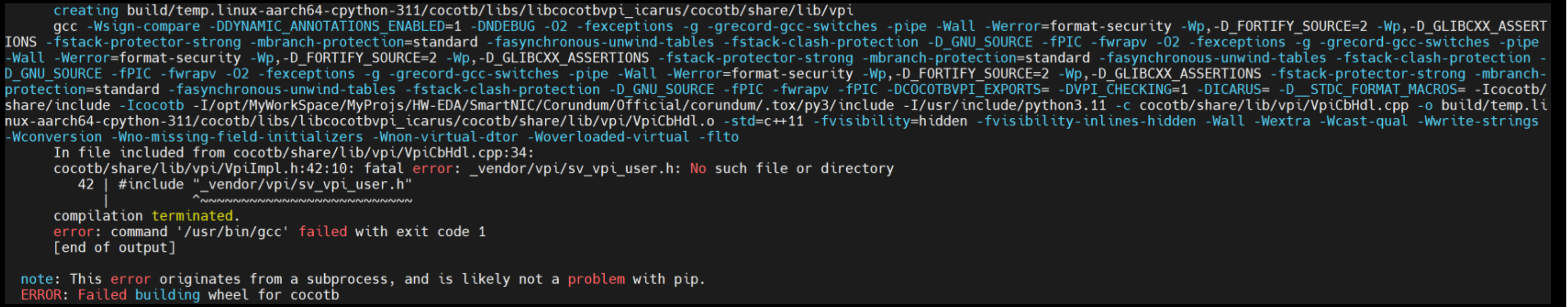
1.1.1 Run by tox

- Src (master branch, last commit: c708bc45cd0d5b44274d238dd9fadd16335f337d ~Dec 6, 2022)



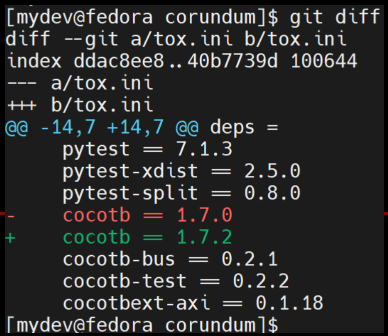
```
[mydev@fedora corundum]$ tox
py3 create: /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum/.tox/py3
py3 installdeps: pytest == 7.1.3, pytest-xdist == 2.5.0, pytest-split == 0.8.0, cocotb == 1.7.0, cocotb-bus == 0.2.1, cocotb-test == 0.2.2, cocotbext-axi == 0.1.18, cocotbext-eth == 0.1.18,
 cocotbext-pcie == 0.2.10, scapy == 2.4.5
ERROR: invocation failed (exit code 1), logfile: /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum/.tox/py3/log/py3-1.log
========================================================================================== log start ==========================================================================================
Collecting pytest==7.1.3
  Downloading pytest-7.1.3-py3-none-any.whl (298 kB)
     ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 298.2/298.2 kB 194.7 kB/s eta 0:00:00
Collecting pytest-xdist==2.5.0
  Downloading pytest_xdist-2.5.0-py3-none-any.whl (41 kB)
     ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 41.7/41.7 kB 209.2 kB/s eta 0:00:00
Collecting pytest-split==0.8.0
  Downloading pytest_split-0.8.0-py3-none-any.whl (11 kB)
Collecting cocotb==1.7.0
  Downloading cocotb-1.7.0.tar.gz (196 kB)
     ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 196.8/196.8 kB 118.4 kB/s eta 0:00:00
  Installing build dependencies: started
  Installing build dependencies: finished with status 'done'
  Getting requirements to build wheel: started
  Getting requirements to build wheel: finished with status 'done'
  Preparing metadata (pyproject.toml): started
  Preparing metadata (pyproject.toml): finished with status 'done'
Collecting cocotb-bus==0.2.1
  Using cached cocotb-bus-0.2.1.tar.gz (28 kB)
  Installing build dependencies: started
  Installing build dependencies: finished with status 'done'
  Getting requirements to build wheel: started
  Getting requirements to build wheel: finished with status 'done'
  Preparing metadata (pyproject.toml): started
  Preparing metadata (pyproject.toml): finished with status 'done'
Collecting cocotb-test==0.2.2
  Downloading cocotb-test-0.2.2.tar.gz (16 kB)
  Preparing metadata (setup.py): started
  Preparing metadata (setup.py): finished with status 'done'
```

...

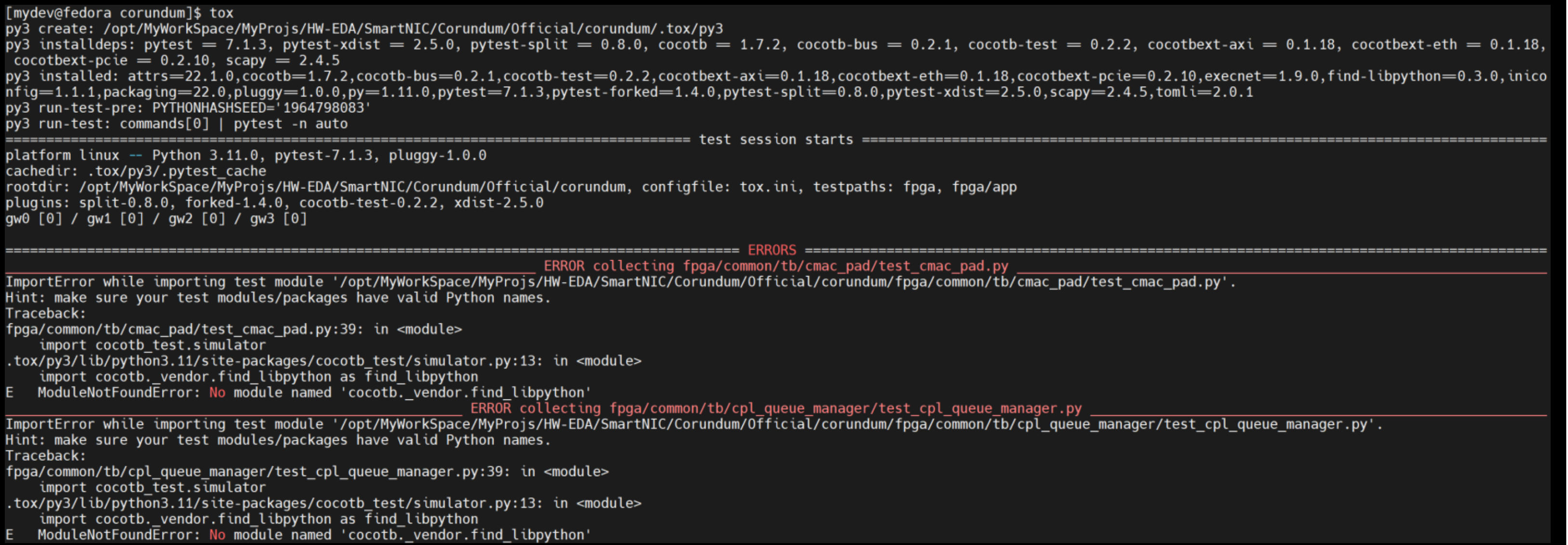


```
      creating build/temp.linux-aarch64-cpython-311/cocotb/libs/libcocotbvpi_icarus/cocotb/share/lib/vpi
      gcc -Wsign-compare -DDYNAMIC_ANNOTATIONS_ENABLED=1 -DNDEBUG -O2 -fexceptions -g -grecord-gcc-switches -pipe -Wall -Werror=format-security -Wp,-D_FORTIFY_SOURCE=2 -Wp,-D_GLIBCXX_ASSERT
IONS -fstack-protector-strong -mbranch-protection=standard -fasynchronous-unwind-tables -fstack-clash-protection -D_GNU_SOURCE -fPIC -fwrapv -O2 -fexceptions -g -grecord-gcc-switches -pipe
-Wall -Werror=format-security -Wp,-D_FORTIFY_SOURCE=2 -Wp,-D_GLIBCXX_ASSERTIONS -fstack-protector-strong -mbranch-protection=standard -fasynchronous-unwind-tables -fstack-clash-protection -
D_GNU_SOURCE -fPIC -fwrapv -O2 -fexceptions -g -grecord-gcc-switches -pipe -Wall -Werror=format-security -Wp,-D_FORTIFY_SOURCE=2 -Wp,-D_GLIBCXX_ASSERTIONS -fstack-protector-strong -mbranch-
protection=standard -fasynchronous-unwind-tables -fstack-clash-protection -D_GNU_SOURCE -fPIC -fwrapv -fPIC -DCOCOTBVPI_EXPORTS= -DVPI_CHECKING=1 -DICARUS= -D__STDC_FORMAT_MACROS= -Icocotb/
share/include -Icocotb -I/opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum/.tox/py3/include -I/usr/include/python3.11 -c cocotb/share/lib/vpi/VpiCbHdl.cpp -o build/temp.li
nux-aarch64-cpython-311/cocotb/libs/libcocotbvpi_icarus/cocotb/share/lib/vpi/VpiCbHdl.o -std=c++11 -fvisibility=hidden -fvisibility-inlines-hidden -Wall -Wextra -Wcast-qual -Wwrite-strings
-Wconversion -Wno-missing-field-initializers -Wnon-virtual-dtor -Woverloaded-virtual -flto
      In file included from cocotb/share/lib/vpi/VpiCbHdl.cpp:34:
      cocotb/share/lib/vpi/VpiImpl.h:42:10: fatal error: _vendor/vpi/sv_vpi_user.h: No such file or directory
         42 | #include "_vendor/vpi/sv_vpi_user.h"
            |          ^~~~~~~~~~~~~~~~~~~~~~~~~~~
      compilation terminated.
      error: command '/usr/bin/gcc' failed with exit code 1
      [end of output]

  note: This error originates from a subprocess, and is likely not a problem with pip.
  ERROR: Failed building wheel for cocotb
```

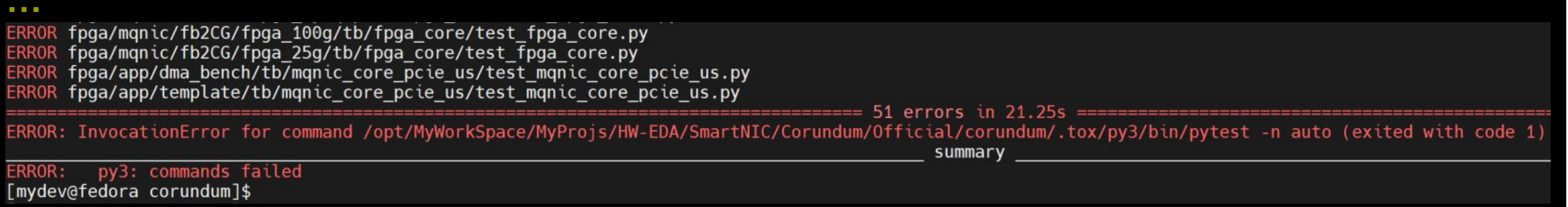
apply a workaround:



```
[mydev@fedora corundum]$ git diff
diff --git a/tox.ini b/tox.ini
index ddac8ee8..40b7739d 100644
--- a/tox.ini
+++ b/tox.ini
@@ -14,7 +14,7 @@ deps =
     pytest == 7.1.3
     pytest-xdist == 2.5.0
     pytest-split == 0.8.0
-    cocotb == 1.7.0
+    cocotb == 1.7.2
     cocotb-bus == 0.2.1
     cocotb-test == 0.2.2
     cocotbext-axi == 0.1.18
[mydev@fedora corundum]$
```

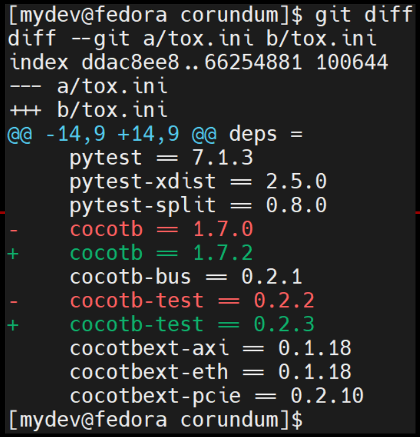


```
[mydev@fedora corundum]$ tox
py3 create: /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum/.tox/py3
py3 installdeps: pytest == 7.1.3, pytest-xdist == 2.5.0, pytest-split == 0.8.0, cocotb == 1.7.2, cocotb-bus == 0.2.1, cocotb-test == 0.2.2, cocotbext-axi == 0.1.18, cocotbext-eth == 0.1.18,
 cocotbext-pcie == 0.2.10, scapy == 2.4.5
py3 installed: attrs==22.1.0,cocotb==1.7.2,cocotb-bus==0.2.1,cocotb-test==0.2.2,cocotbext-axi==0.1.18,cocotbext-eth==0.1.18,cocotbext-pcie==0.2.10,execnet==1.9.0,find-libpython==0.3.0,inico
nfig==1.1.1,packaging==22.0,pluggy==1.0.0,py==1.11.0,pytest==7.1.3,pytest-forked==1.4.0,pytest-split==0.8.0,pytest-xdist==2.5.0,scapy==2.4.5,tomli==2.0.1
py3 run-test-pre: PYTHONHASHSEED='1964798083'
py3 run-test: commands[0] | pytest -n auto
=============================================================================== test session starts ================================================================================
platform linux -- Python 3.11.0, pytest-7.1.3, pluggy-1.0.0
cachedir: .tox/py3/.pytest_cache
rootdir: /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum, configfile: tox.ini, testpaths: fpga, fpga/app
plugins: split-0.8.0, forked-1.4.0, cocotb-test-0.2.2, xdist-2.5.0
gw0 [0] / gw1 [0] / gw2 [0] / gw3 [0]

===================================================================================== ERRORS =====================================================================================
_____________________________________________________________ ERROR collecting fpga/common/tb/cmac_pad/test_cmac_pad.py ______________________________________________________________
ImportError while importing test module '/opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum/fpga/common/tb/cmac_pad/test_cmac_pad.py'.
Hint: make sure your test modules/packages have valid Python names.
Traceback:
fpga/common/tb/cmac_pad/test_cmac_pad.py:39: in <module>
    import cocotb_test.simulator
.tox/py3/lib/python3.11/site-packages/cocotb_test/simulator.py:13: in <module>
    import cocotb._vendor.find_libpython as find_libpython
E   ModuleNotFoundError: No module named 'cocotb._vendor.find_libpython'
_____________________________________________________ ERROR collecting fpga/common/tb/cpl_queue_manager/test_cpl_queue_manager.py ______________________________________________________
ImportError while importing test module '/opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum/fpga/common/tb/cpl_queue_manager/test_cpl_queue_manager.py'.
Hint: make sure your test modules/packages have valid Python names.
Traceback:
fpga/common/tb/cpl_queue_manager/test_cpl_queue_manager.py:39: in <module>
    import cocotb_test.simulator
.tox/py3/lib/python3.11/site-packages/cocotb_test/simulator.py:13: in <module>
    import cocotb._vendor.find_libpython as find_libpython
E   ModuleNotFoundError: No module named 'cocotb._vendor.find_libpython'
```

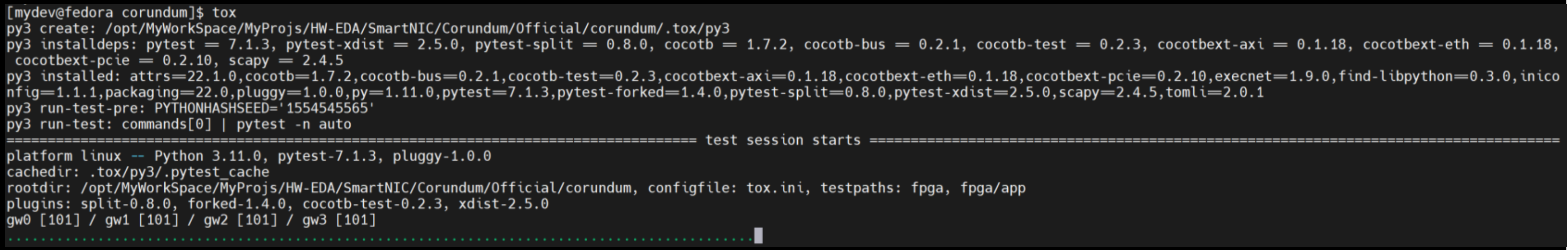


```
...
ERROR fpga/mqnic/fb2CG/fpga_100g/tb/fpga_core/test_fpga_core.py
ERROR fpga/mqnic/fb2CG/fpga_25g/tb/fpga_core/test_fpga_core.py
ERROR fpga/app/dma_bench/tb/mqnic_core_pcie_us/test_mqnic_core_pcie_us.py
ERROR fpga/app/template/tb/mqnic_core_pcie_us/test_mqnic_core_pcie_us.py
=============================================================== 51 errors in 21.25s ================================================================
ERROR: InvocationError for command /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum/.tox/py3/bin/pytest -n auto (exited with code 1)
_____________________________________________________________________ summary ______________________________________________________________________
ERROR:   py3: commands failed
[mydev@fedora corundum]$
```

apply another workaround:



```
[mydev@fedora corundum]$ git diff
diff --git a/tox.ini b/tox.ini
index ddac8ee8..66254881 100644
--- a/tox.ini
+++ b/tox.ini
@@ -14,9 +14,9 @@ deps =
     pytest == 7.1.3
     pytest-xdist == 2.5.0
     pytest-split == 0.8.0
-    cocotb == 1.7.0
+    cocotb == 1.7.2
     cocotb-bus == 0.2.1
-    cocotb-test == 0.2.2
+    cocotb-test == 0.2.3
     cocotbext-axi == 0.1.18
     cocotbext-eth == 0.1.18
     cocotbext-pcie == 0.2.10
[mydev@fedora corundum]$
```

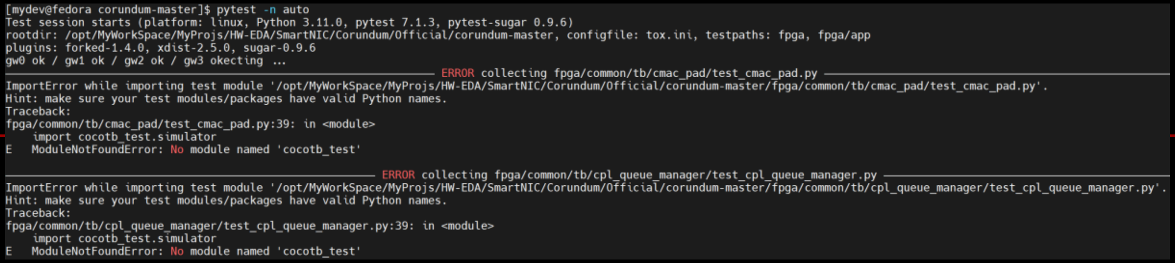


```
[mydev@fedora corundum]$ tox
py3 create: /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum/.tox/py3
py3 installdeps: pytest == 7.1.3, pytest-xdist == 2.5.0, pytest-split == 0.8.0, cocotb == 1.7.2, cocotb-bus == 0.2.1, cocotb-test == 0.2.3, cocotbext-axi == 0.1.18, cocotbext-eth == 0.1.18,
 cocotbext-pcie == 0.2.10, scapy == 2.4.5
py3 installed: attrs==22.1.0,cocotb==1.7.2,cocotb-bus==0.2.1,cocotb-test==0.2.3,cocotbext-axi==0.1.18,cocotbext-eth==0.1.18,cocotbext-pcie==0.2.10,execnet==1.9.0,find-libpython==0.3.0,inico
nfig==1.1.1,packaging==22.0,pluggy==1.0.0,py==1.11.0,pytest==7.1.3,pytest-forked==1.4.0,pytest-split==0.8.0,pytest-xdist==2.5.0,scapy==2.4.5,tomli==2.0.1
py3 run-test-pre: PYTHONHASHSEED='1554545565'
py3 run-test: commands[0] | pytest -n auto
================================================================================= test session starts =================================================================================
platform linux -- Python 3.11.0, pytest-7.1.3, pluggy-1.0.0
cachedir: .tox/py3/.pytest_cache
rootdir: /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum, configfile: tox.ini, testpaths: fpga, fpga/app
plugins: split-0.8.0, forked-1.4.0, cocotb-test-0.2.3, xdist-2.5.0
gw0 [101] / gw1 [101] / gw2 [101] / gw3 [101]
.........................................................................................
```

Test program exited quietly after successfully running most of the cases without explicit error info(seems caused by some time out) after running over a day, we are investigating the root cause…

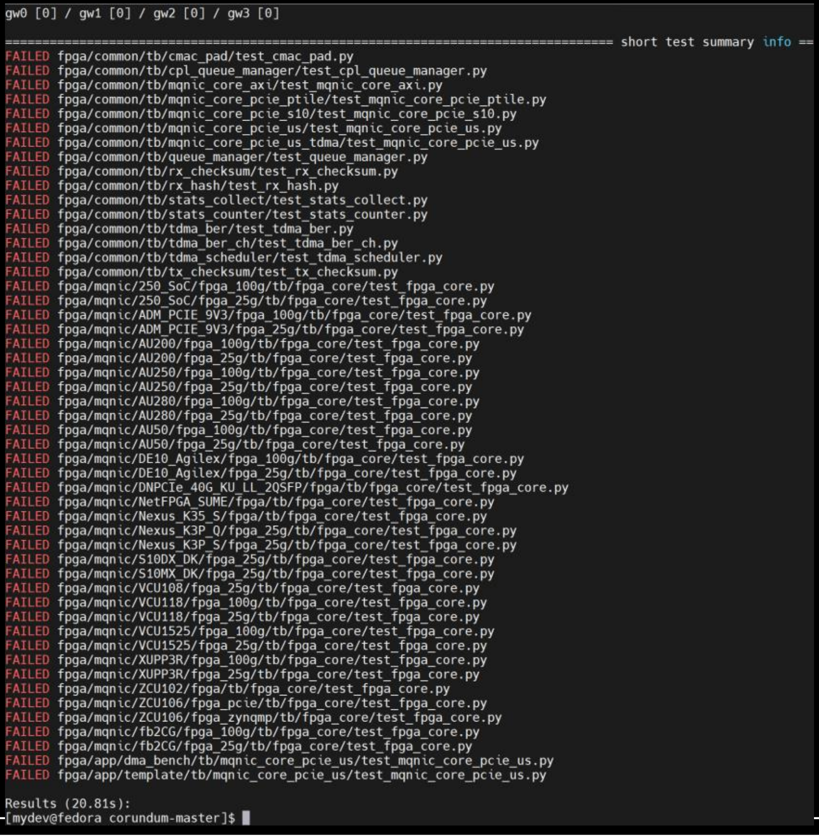
1.1.2 Run without tox

- **Src** (master branch, last commit: c708bc45cd0d5b44274d238dd9fadd16335f337d ~Dec 6, 2022)

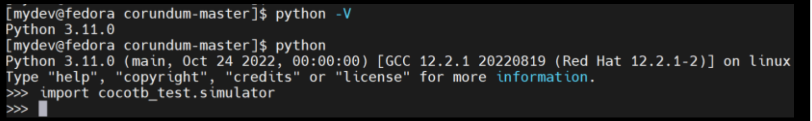


```
[mydev@fedora corundum-master]$ pytest -n auto
Test session starts (platform: linux, Python 3.11.0, pytest 7.1.3, pytest-sugar 0.9.6)
rootdir: /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum-master, configfile: tox.ini, testpaths: fpga, fpga/app
plugins: forked-1.4.0, xdist-2.5.0, sugar-0.9.6
gw0 ok / gw1 ok / gw2 ok / gw3 okecting ...
──────────────────────────────── ERROR collecting fpga/common/tb/cmac_pad/test_cmac_pad.py ────────────────────────────────
ImportError while importing test module '/opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum-master/fpga/common/tb/cmac_pad/test_cmac_pad.py'.
Hint: make sure your test modules/packages have valid Python names.
Traceback:
fpga/common/tb/cmac_pad/test_cmac_pad.py:39: in <module>
    import cocotb_test.simulator
E   ModuleNotFoundError: No module named 'cocotb_test'

────────────────────────── ERROR collecting fpga/common/tb/cpl_queue_manager/test_cpl_queue_manager.py ──────────────────────────
ImportError while importing test module '/opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum-master/fpga/common/tb/cpl_queue_manager/test_cpl_queue_manager.py'.
Hint: make sure your test modules/packages have valid Python names.
Traceback:
fpga/common/tb/cpl_queue_manager/test_cpl_queue_manager.py:39: in <module>
    import cocotb_test.simulator
E   ModuleNotFoundError: No module named 'cocotb_test'
```

...

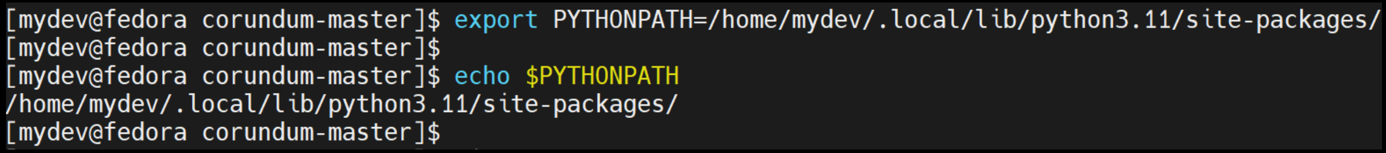


```
gw0 [0] / gw1 [0] / gw2 [0] / gw3 [0]

=============================================================================== short test summary info ==
FAILED fpga/common/tb/cmac_pad/test_cmac_pad.py
FAILED fpga/common/tb/cpl_queue_manager/test_cpl_queue_manager.py
FAILED fpga/common/tb/mqnic_core_axi/test_mqnic_core_axi.py
FAILED fpga/common/tb/mqnic_core_pcie_ptile/test_mqnic_core_pcie_ptile.py
FAILED fpga/common/tb/mqnic_core_pcie_s10/test_mqnic_core_pcie_s10.py
FAILED fpga/common/tb/mqnic_core_pcie_us/test_mqnic_core_pcie_us.py
FAILED fpga/common/tb/mqnic_core_pcie_us_tdma/test_mqnic_core_pcie_us.py
FAILED fpga/common/tb/queue_manager/test_queue_manager.py
FAILED fpga/common/tb/rx_checksum/test_rx_checksum.py
FAILED fpga/common/tb/rx_hash/test_rx_hash.py
FAILED fpga/common/tb/stats_collect/test_stats_collect.py
FAILED fpga/common/tb/stats_counter/test_stats_counter.py
FAILED fpga/common/tb/tdma_ber/test_tdma_ber.py
FAILED fpga/common/tb/tdma_ber_ch/test_tdma_ber_ch.py
FAILED fpga/common/tb/tdma_scheduler/test_tdma_scheduler.py
FAILED fpga/common/tb/tx_checksum/test_tx_checksum.py
FAILED fpga/mqnic/250_SoC/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/250_SoC/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/ADM_PCIE_9V3/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/ADM_PCIE_9V3/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/AU200/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/AU200/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/AU250/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/AU250/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/AU280/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/AU280/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/AU50/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/AU50/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/DE10_Agilex/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/DE10_Agilex/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/DNPCIe_40G_KU_LL_2QSFP/fpga/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/NetFPGA_SUME/fpga/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/Nexus_K35_S/fpga/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/Nexus_K3P_Q/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/Nexus_K3P_S/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/S10DX_DK/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/S10MX_DK/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/VCU108/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/VCU118/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/VCU118/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/VCU1525/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/VCU1525/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/XUPP3R/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/XUPP3R/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/ZCU102/fpga/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/ZCU106/fpga_pcie/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/ZCU106/fpga_zynqmp/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/fb2CG/fpga_100g/tb/fpga_core/test_fpga_core.py
FAILED fpga/mqnic/fb2CG/fpga_25g/tb/fpga_core/test_fpga_core.py
FAILED fpga/app/dma_bench/tb/mqnic_core_pcie_us/test_mqnic_core_pcie_us.py
FAILED fpga/app/template/tb/mqnic_core_pcie_us/test_mqnic_core_pcie_us.py

Results (20.81s):
[mydev@fedora corundum-master]$ █
```

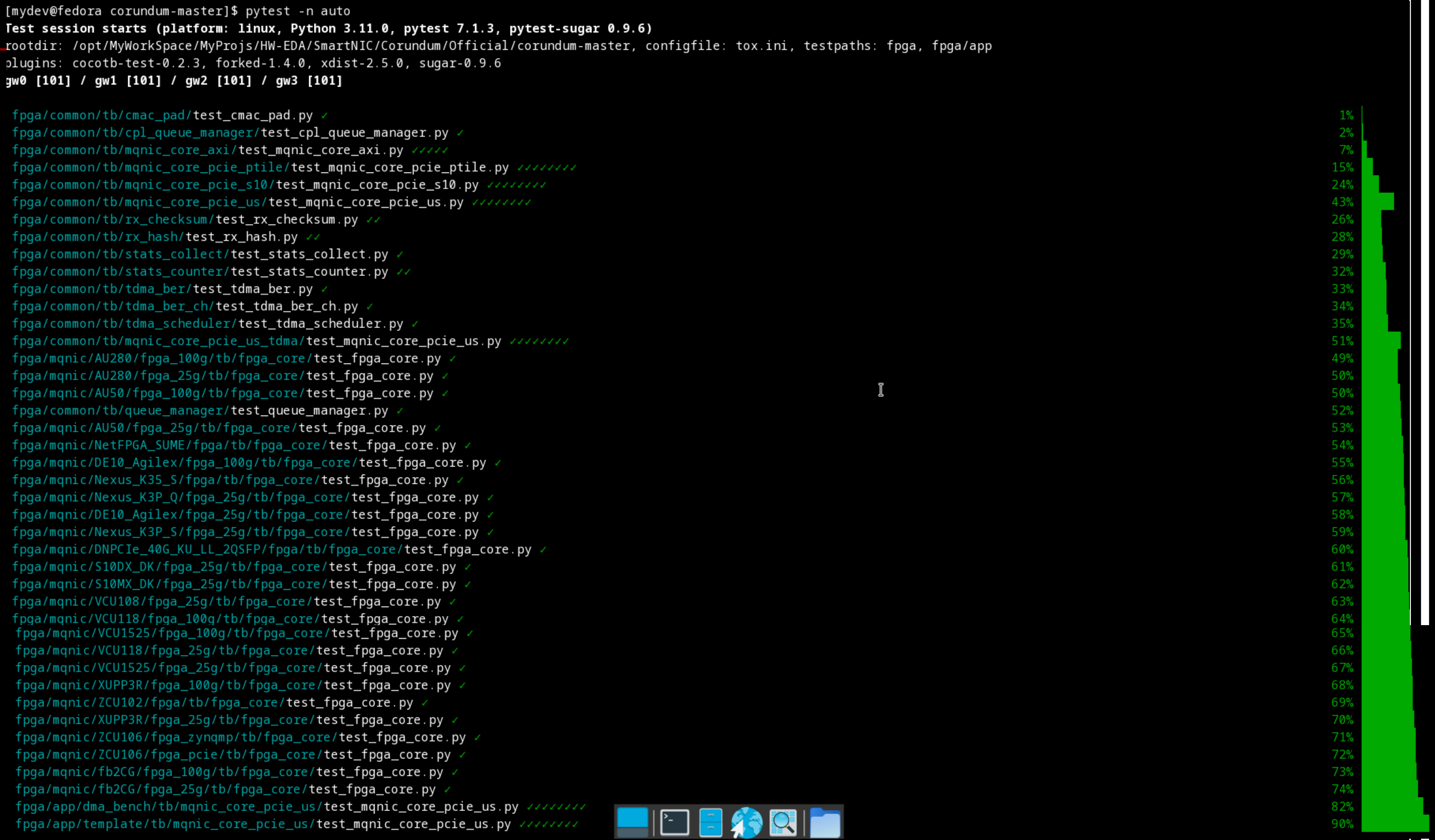


```
[mydev@fedora corundum-master]$ python -V
Python 3.11.0
[mydev@fedora corundum-master]$ python
Python 3.11.0 (main, Oct 24 2022, 00:00:00) [GCC 12.2.1 20220819 (Red Hat 12.2.1-2)] on linux
Type "help", "copyright", "credits" or "license" for more information.
>>> import cocotb_test.simulator
>>> █
```

set PYTHONPATH and rerun the tests:



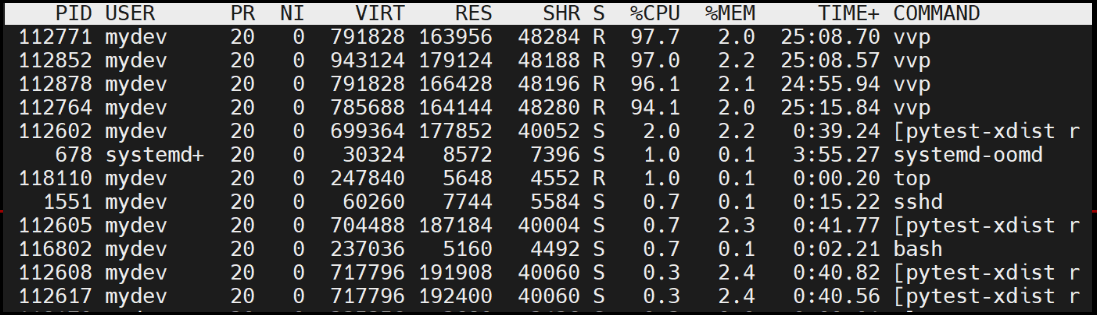
```
[mydev@fedora corundum-master]$ export PYTHONPATH=/home/mydev/.local/lib/python3.11/site-packages/
[mydev@fedora corundum-master]$
[mydev@fedora corundum-master]$ echo $PYTHONPATH
/home/mydev/.local/lib/python3.11/site-packages/
[mydev@fedora corundum-master]$
```



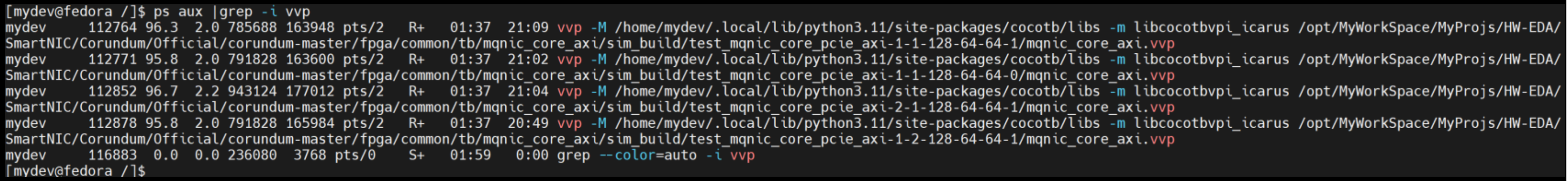
```
[mydev@fedora corundum-master]$ pytest -n auto
Test session starts (platform: linux, Python 3.11.0, pytest 7.1.3, pytest-sugar 0.9.6)
rootdir: /opt/MyWorkSpace/MyProjs/HW-EDA/SmartNIC/Corundum/Official/corundum-master, configfile: tox.ini, testpaths: fpga, fpga/app
plugins: cocotb-test-0.2.3, forked-1.4.0, xdist-2.5.0, sugar-0.9.6
gw0 [101] / gw1 [101] / gw2 [101] / gw3 [101]

 fpga/common/tb/cmac_pad/test_cmac_pad.py ✓                                                          1%
 fpga/common/tb/cpl_queue_manager/test_cpl_queue_manager.py ✓                                        2%
 fpga/common/tb/mqnic_core_axi/test_mqnic_core_axi.py ✓✓✓✓✓                                          7%
 fpga/common/tb/mqnic_core_pcie_ptile/test_mqnic_core_pcie_ptile.py ✓✓✓✓✓✓✓✓                        15%
 fpga/common/tb/mqnic_core_pcie_s10/test_mqnic_core_pcie_s10.py ✓✓✓✓✓✓✓✓                            24%
 fpga/common/tb/mqnic_core_pcie_us/test_mqnic_core_pcie_us.py ✓✓✓✓✓✓✓✓                              43%
 fpga/common/tb/rx_checksum/test_rx_checksum.py ✓✓                                                  26%
 fpga/common/tb/rx_hash/test_rx_hash.py ✓✓                                                          28%
 fpga/common/tb/stats_collect/test_stats_collect.py ✓                                               29%
 fpga/common/tb/stats_counter/test_stats_counter.py ✓✓                                              32%
 fpga/common/tb/tdma_ber/test_tdma_ber.py ✓                                                         33%
 fpga/common/tb/tdma_ber_ch/test_tdma_ber_ch.py ✓                                                   34%
 fpga/common/tb/tdma_scheduler/test_tdma_scheduler.py ✓                                             35%
 fpga/common/tb/mqnic_core_pcie_us_tdma/test_mqnic_core_pcie_us.py ✓✓✓✓✓✓✓✓                         51%
 fpga/mqnic/AU280/fpga_100g/tb/fpga_core/test_fpga_core.py ✓                                        49%
 fpga/mqnic/AU280/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                         50%
 fpga/mqnic/AU50/fpga_100g/tb/fpga_core/test_fpga_core.py ✓                                         50%
 fpga/common/tb/queue_manager/test_queue_manager.py ✓                                               52%
 fpga/mqnic/AU50/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                          53%
 fpga/mqnic/NetFPGA_SUME/fpga/tb/fpga_core/test_fpga_core.py ✓                                      54%
 fpga/mqnic/DE10_Agilex/fpga_100g/tb/fpga_core/test_fpga_core.py ✓                                  55%
 fpga/mqnic/Nexus_K35_S/fpga/tb/fpga_core/test_fpga_core.py ✓                                       56%
 fpga/mqnic/Nexus_K3P_Q/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                   57%
 fpga/mqnic/DE10_Agilex/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                   58%
 fpga/mqnic/Nexus_K3P_S/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                   59%
 fpga/mqnic/DNPCIe_40G_KU_LL_2QSFP/fpga/tb/fpga_core/test_fpga_core.py ✓                            60%
 fpga/mqnic/S10DX_DK/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                      61%
 fpga/mqnic/S10MX_DK/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                      62%
 fpga/mqnic/VCU108/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                        63%
 fpga/mqnic/VCU118/fpga_100g/tb/fpga_core/test_fpga_core.py ✓                                       64%
 fpga/mqnic/VCU1525/fpga_100g/tb/fpga_core/test_fpga_core.py ✓                                      65%
 fpga/mqnic/VCU118/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                        66%
 fpga/mqnic/VCU1525/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                       67%
 fpga/mqnic/XUPP3R/fpga_100g/tb/fpga_core/test_fpga_core.py ✓                                       68%
 fpga/mqnic/ZCU102/fpga/tb/fpga_core/test_fpga_core.py ✓                                            69%
 fpga/mqnic/XUPP3R/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                        70%
 fpga/mqnic/ZCU106/fpga_zynqmp/tb/fpga_core/test_fpga_core.py ✓                                     71%
 fpga/mqnic/ZCU106/fpga_pcie/tb/fpga_core/test_fpga_core.py ✓                                       72%
 fpga/mqnic/fb2CG/fpga_100g/tb/fpga_core/test_fpga_core.py ✓                                        73%
 fpga/mqnic/fb2CG/fpga_25g/tb/fpga_core/test_fpga_core.py ✓                                         74%
 fpga/app/dma_bench/tb/mqnic_core_pcie_us/test_mqnic_core_pcie_us.py ✓✓✓✓✓✓✓✓                       82%
 fpga/app/template/tb/mqnic_core_pcie_us/test_mqnic_core_pcie_us.py ✓✓✓✓✓✓✓✓                        90%
```

Test program exited quietly without explicit error info as previous section while reaching 90%, working on it…

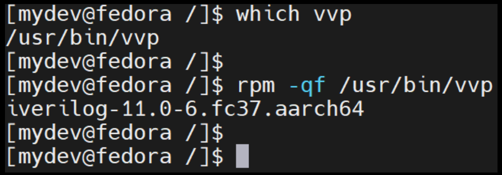
check:



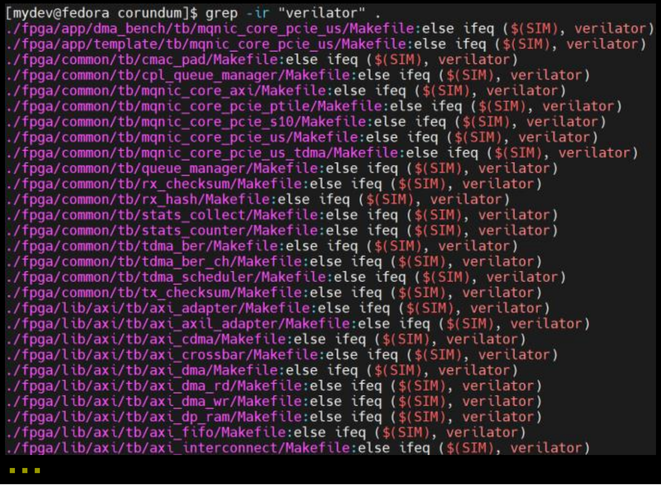
```
   PID USER      PR  NI    VIRT    RES    SHR S  %CPU  %MEM     TIME+ COMMAND
112771 mydev     20   0  791828 163956  48284 R  97.7   2.0  25:08.70 vvp
112852 mydev     20   0  943124 179124  48188 R  97.0   2.2  25:08.57 vvp
112878 mydev     20   0  791828 166428  48196 R  96.1   2.1  24:55.94 vvp
112764 mydev     20   0  785688 164144  48280 R  94.1   2.0  25:15.84 vvp
112602 mydev     20   0  699364 177852  40052 S   2.0   2.2   0:39.24 [pytest-xdist r
   678 systemd+  20   0   30324   8572   7396 S   1.0   0.1   3:55.27 systemd-oomd
118110 mydev     20   0  247840   5648   4552 R   1.0   0.1   0:00.20 top
  1551 mydev     20   0   60260   7744   5584 S   0.7   0.1   0:15.22 sshd
112605 mydev     20   0  704488 187184  40004 S   0.7   2.3   0:41.77 [pytest-xdist r
116802 mydev     20   0  237036   5160   4492 S   0.7   0.1   0:02.21 bash
112608 mydev     20   0  717796 191908  40060 S   0.3   2.4   0:40.82 [pytest-xdist r
112617 mydev     20   0  717796 192400  40060 S   0.3   2.4   0:40.56 [pytest-xdist r
```



```
[mydev@fedora /]$ ps aux |grep -i vvp
mydev     112764 96.3  2.0 785688 163948 pts/2   R+   01:37  21:09 vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus /opt/MyWorkSpace/MyProjs/HW-EDA/
SmartNIC/Corundum/Official/corundum-master/fpga/common/tb/mqnic_core_axi/sim_build/test_mqnic_core_pcie_axi-1-1-128-64-64-1/mqnic_core_axi.vvp
mydev     112771 95.8  2.0 791828 163600 pts/2   R+   01:37  21:02 vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus /opt/MyWorkSpace/MyProjs/HW-EDA/
SmartNIC/Corundum/Official/corundum-master/fpga/common/tb/mqnic_core_axi/sim_build/test_mqnic_core_pcie_axi-1-1-128-64-64-0/mqnic_core_axi.vvp
mydev     112852 96.7  2.2 943124 177012 pts/2   R+   01:37  21:04 vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus /opt/MyWorkSpace/MyProjs/HW-EDA/
SmartNIC/Corundum/Official/corundum-master/fpga/common/tb/mqnic_core_axi/sim_build/test_mqnic_core_pcie_axi-2-1-128-64-64-1/mqnic_core_axi.vvp
mydev     112878 95.8  2.0 791828 165984 pts/2   R+   01:37  20:49 vvp -M /home/mydev/.local/lib/python3.11/site-packages/cocotb/libs -m libcocotbvpi_icarus /opt/MyWorkSpace/MyProjs/HW-EDA/
SmartNIC/Corundum/Official/corundum-master/fpga/common/tb/mqnic_core_axi/sim_build/test_mqnic_core_pcie_axi-1-2-128-64-64-1/mqnic_core_axi.vvp
mydev     116883  0.0  0.0 236080  3768 pts/0    S+   01:59   0:00 grep --color=auto -i vvp
[mydev@fedora /]$
```

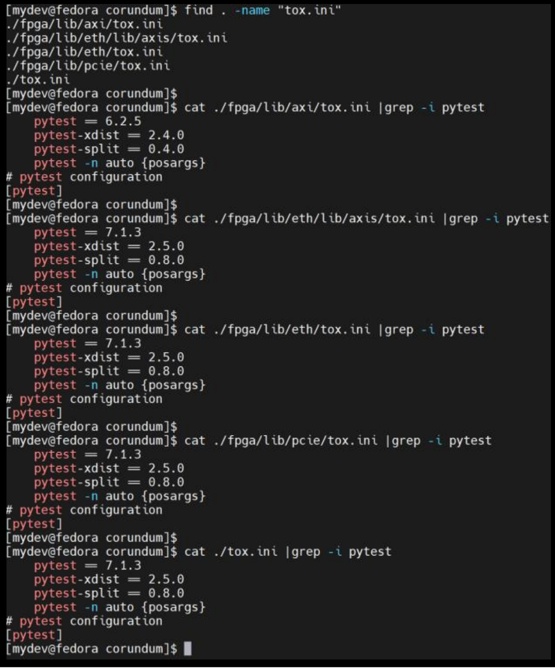


```
[mydev@fedora /]$ which vvp
/usr/bin/vvp
[mydev@fedora /]$
[mydev@fedora /]$ rpm -qf /usr/bin/vvp
iverilog-11.0-6.fc37.aarch64
[mydev@fedora /]$
[mydev@fedora /]$ 
```



```
[mydev@fedora corundum]$ grep -ir "verilator" .
./fpga/app/dma_bench/tb/mqnic_core_pcie_us/Makefile:else ifeq ($(SIM), verilator)
./fpga/app/template/tb/mqnic_core_pcie_us/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/cmac_pad/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/cpl_queue_manager/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/mqnic_core_axi/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/mqnic_core_pcie_ptile/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/mqnic_core_pcie_s10/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/mqnic_core_pcie_us/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/mqnic_core_pcie_us_tdma/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/queue_manager/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/rx_checksum/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/rx_hash/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/stats_collect/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/stats_counter/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/tdma_ber/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/tdma_ber_ch/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/tdma_scheduler/Makefile:else ifeq ($(SIM), verilator)
./fpga/common/tb/tx_checksum/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_adapter/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_axil_adapter/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_cdma/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_crossbar/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_dma/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_dma_rd/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_dma_wr/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_dp_ram/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_fifo/Makefile:else ifeq ($(SIM), verilator)
./fpga/lib/axi/tb/axi_interconnect/Makefile:else ifeq ($(SIM), verilator)
```

...



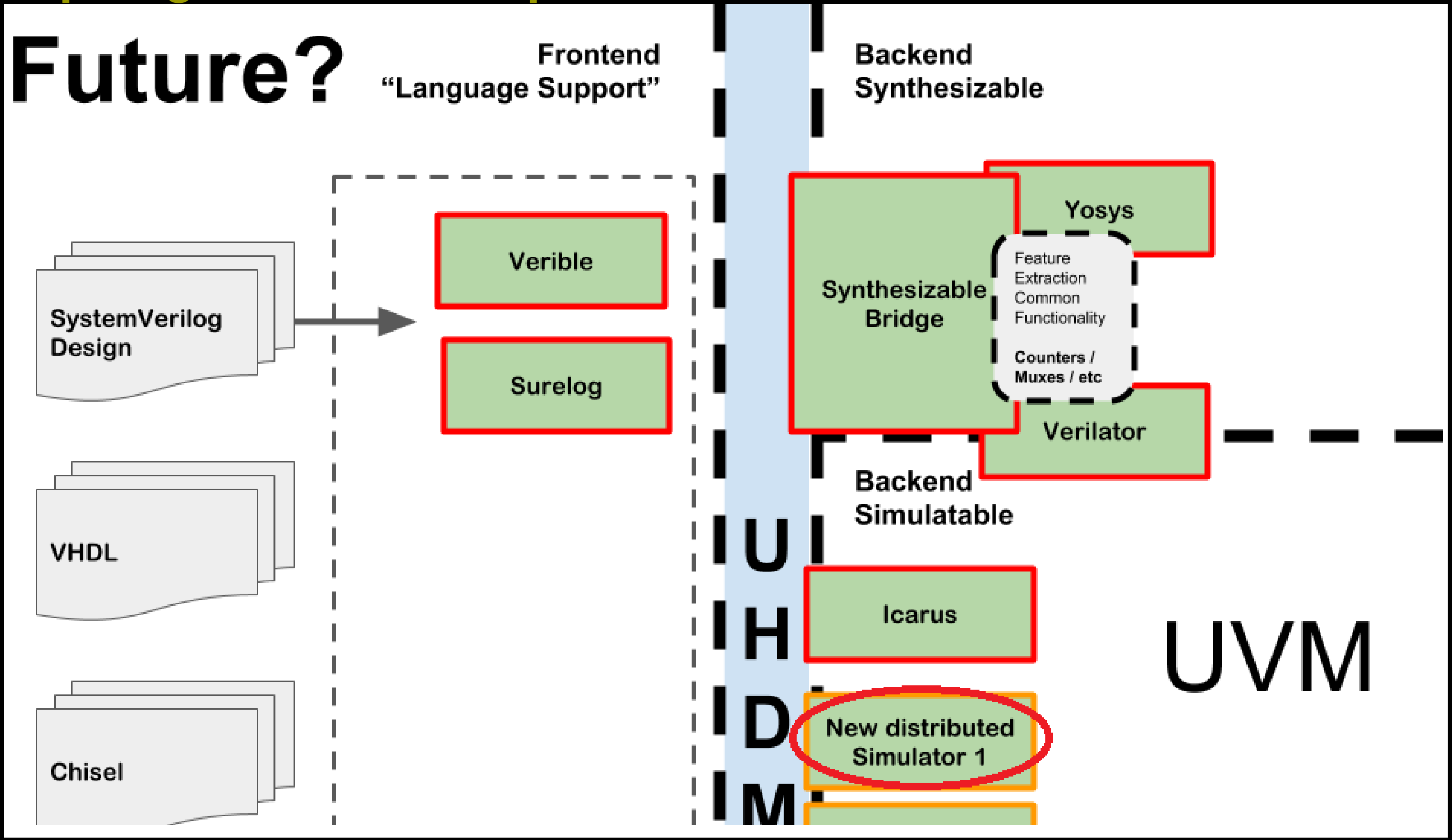
```
[mydev@fedora corundum]$ find . -name "tox.ini"
./fpga/lib/axi/tox.ini
./fpga/lib/eth/lib/axis/tox.ini
./fpga/lib/eth/tox.ini
./fpga/lib/pcie/tox.ini
./tox.ini
[mydev@fedora corundum]$
[mydev@fedora corundum]$ cat ./fpga/lib/axi/tox.ini |grep -i pytest
    pytest == 6.2.5
    pytest-xdist == 2.4.0
    pytest-split == 0.4.0
    pytest -n auto {posargs}
# pytest configuration
[pytest]
[mydev@fedora corundum]$
[mydev@fedora corundum]$ cat ./fpga/lib/eth/lib/axis/tox.ini |grep -i pytest
    pytest == 7.1.3
    pytest-xdist == 2.5.0
    pytest-split == 0.8.0
    pytest -n auto {posargs}
# pytest configuration
[pytest]
[mydev@fedora corundum]$
[mydev@fedora corundum]$ cat ./fpga/lib/eth/tox.ini |grep -i pytest
    pytest == 7.1.3
    pytest-xdist == 2.5.0
    pytest-split == 0.8.0
    pytest -n auto {posargs}
# pytest configuration
[pytest]
[mydev@fedora corundum]$
[mydev@fedora corundum]$ cat ./fpga/lib/pcie/tox.ini |grep -i pytest
    pytest == 7.1.3
    pytest-xdist == 2.5.0
    pytest-split == 0.8.0
    pytest -n auto {posargs}
# pytest configuration
[pytest]
[mydev@fedora corundum]$
[mydev@fedora corundum]$ cat ./tox.ini |grep -i pytest
    pytest == 7.1.3
    pytest-xdist == 2.5.0
    pytest-split == 0.8.0
    pytest -n auto {posargs}
# pytest configuration
[pytest]
[mydev@fedora corundum]$ 
```

IV. Project CocotbD

1) The future of HW Verification

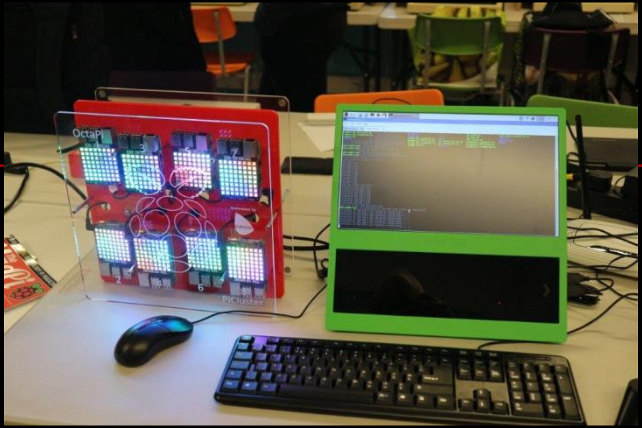
1.1 Distributed Simulation

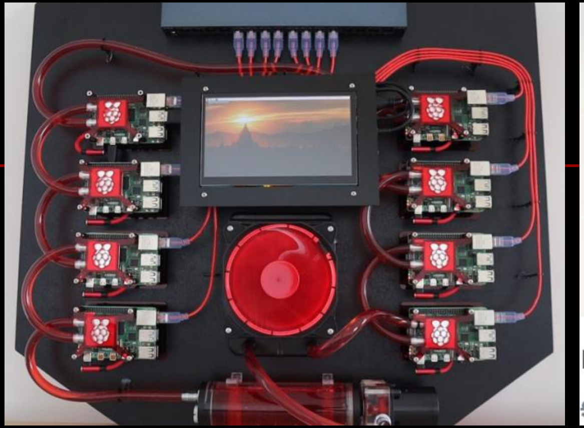
- https://github.com/chipsalliance/UHDM

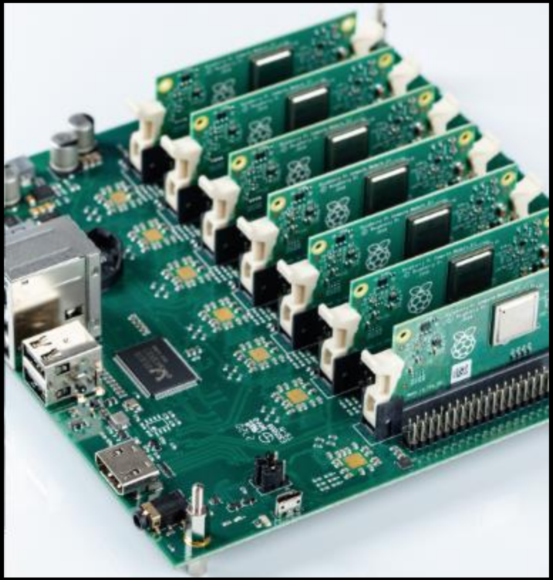


...

1.1.1 RPi Clusters





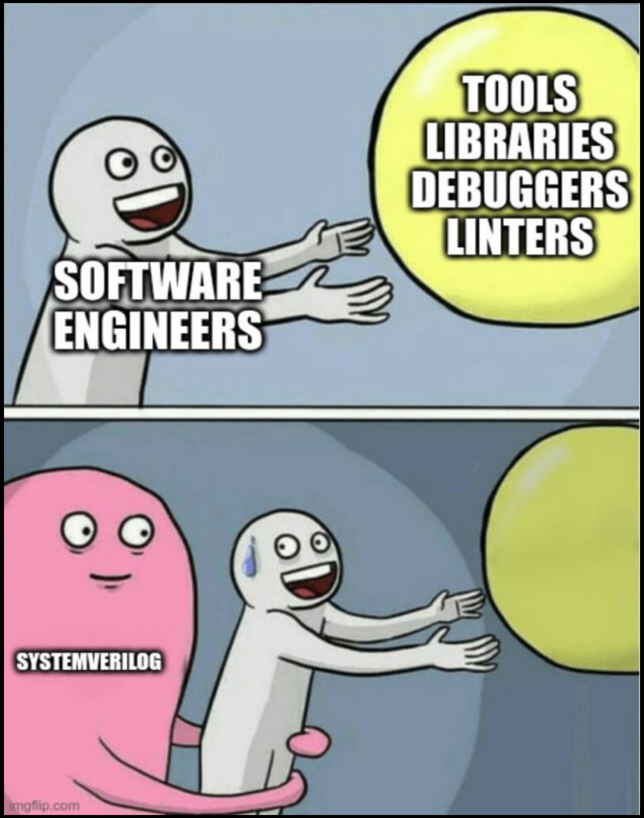


ARGON EON PI NAS
树莓派私有云网络存储机箱
支持SSD和HDD硬盘 | 可编程OLED屏 | 内置时钟模块
EON
航空级铝制外壳 适用于树莓派4B

1.2 Beyond UVM

1.2.1 It's time to thank UVM and say goodbye?

- https://olofkindgren.blogspot.com/2022/10/its-time-to-to-thank-uvm-and-say-goodbye.html



…

1.3 Hardware-assisted Verification

1.3.1 Overview

- https://semiwiki.com/eda/siemens-eda/317651-todays-soc-design-verification-and-validation-require-three-types-of-hardware-assisted-engines/
- https://www.analogictips.com/hardware-assisted-verification-technology-in-the-mainstream/

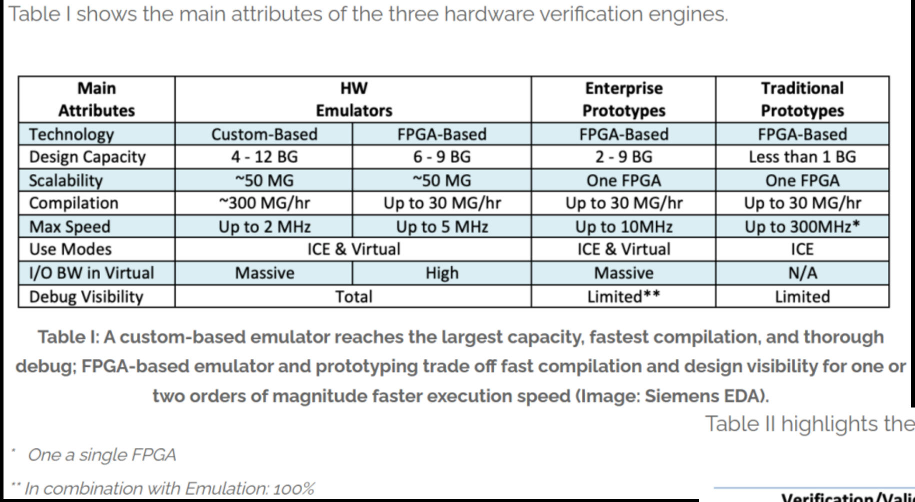


Table I shows the main attributes of the three hardware verification engines.

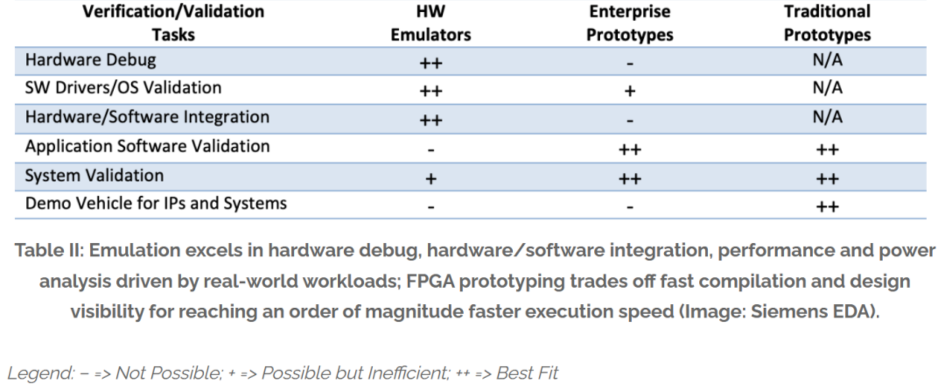
Main Attributes	HW Emulators		Enterprise Prototypes	Traditional Prototypes
Technology	Custom-Based	FPGA-Based	FPGA-Based	FPGA-Based
Design Capacity	4 - 12 BG	6 - 9 BG	2 - 9 BG	Less than 1 BG
Scalability	~50 MG	~50 MG	One FPGA	One FPGA
Compilation	~300 MG/hr	Up to 30 MG/hr	Up to 30 MG/hr	Up to 30 MG/hr
Max Speed	Up to 2 MHz	Up to 5 MHz	Up to 10MHz	Up to 300MHz*
Use Modes	ICE & Virtual		ICE & Virtual	ICE
I/O BW in Virtual	Massive	High	Massive	N/A
Debug Visibility	Total		Limited**	Limited

Table I: A custom-based emulator reaches the largest capacity, fastest compilation, and thorough debug; FPGA-based emulator and prototyping trade off fast compilation and design visibility for one or two orders of magnitude faster execution speed (Image: Siemens EDA).

** One a single FPGA*

*** In combination with Emulation: 100%*

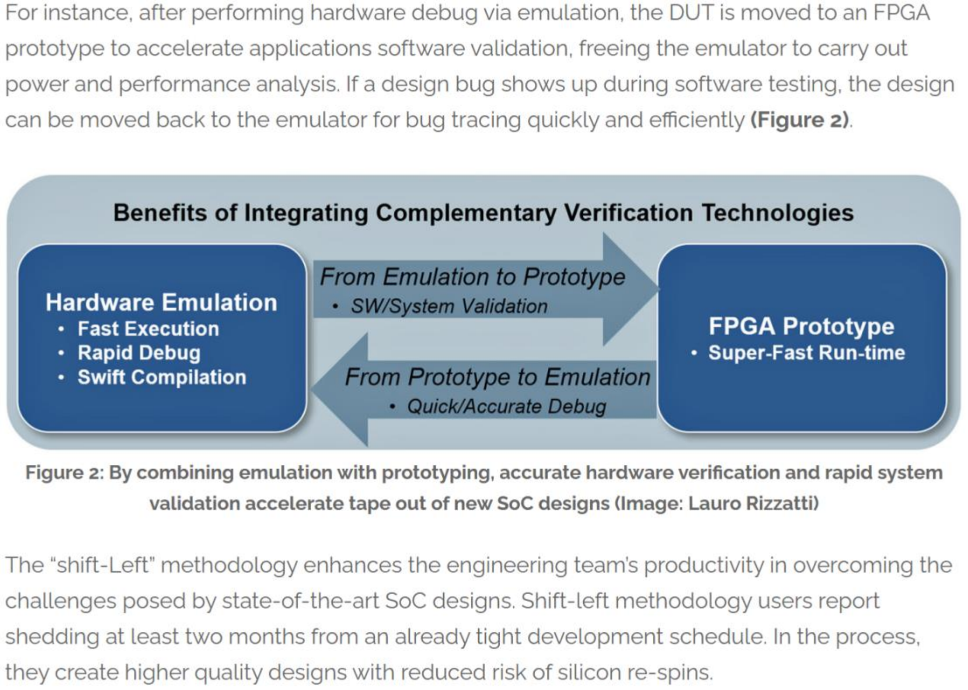
Table II highlights the best fit for each hardware-assisted verification tool.



Verification/Validation Tasks	HW Emulators	Enterprise Prototypes	Traditional Prototypes
Hardware Debug	++	-	N/A
SW Drivers/OS Validation	++	+	N/A
Hardware/Software Integration	++	-	N/A
Application Software Validation	-	++	++
System Validation	+	++	++
Demo Vehicle for IPs and Systems	-	-	++

Table II: Emulation excels in hardware debug, hardware/software integration, performance and power analysis driven by real-world workloads; FPGA prototyping trades off fast compilation and design visibility for reaching an order of magnitude faster execution speed (Image: Siemens EDA).

Legend: – => Not Possible; + => Possible but Inefficient; ++ => Best Fit



For instance, after performing hardware debug via emulation, the DUT is moved to an FPGA prototype to accelerate applications software validation, freeing the emulator to carry out power and performance analysis. If a design bug shows up during software testing, the design can be moved back to the emulator for bug tracing quickly and efficiently **(Figure 2)**.

Figure 2: By combining emulation with prototyping, accurate hardware verification and rapid system validation accelerate tape out of new SoC designs (Image: Lauro Rizzatti)

The "shift-Left" methodology enhances the engineering team's productivity in overcoming the challenges posed by state-of-the-art SoC designs. Shift-left methodology users report shedding at least two months from an already tight development schedule. In the process, they create higher quality designs with reduced risk of silicon re-spins.

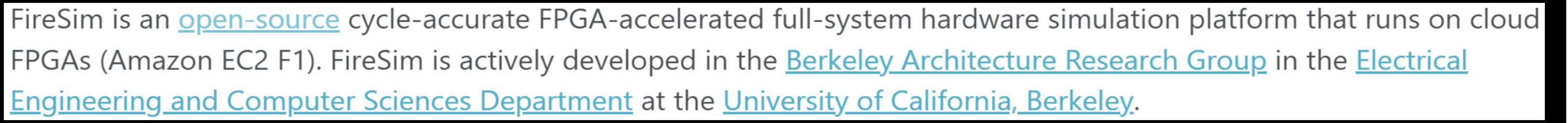
- https://www.cnctimes.com/editorial/siemens-delivers-next-generation-comprehensive-hardware-assisted-verification-system
- https://news.synopsys.com/2022-09-20-Synopsys-Unveils-Industrys-First-Unified-Emulation-and-Prototyping-System-Addressing-Verification-Requirements-Across-the-Chip-Development-Cycle
- https://www.intellectualmarketinsights.com/report/hardware-assisted-verification-market-size-and-trends/imi-001814
- …

1.3.2 FireSim

1.3.2.1 Overview

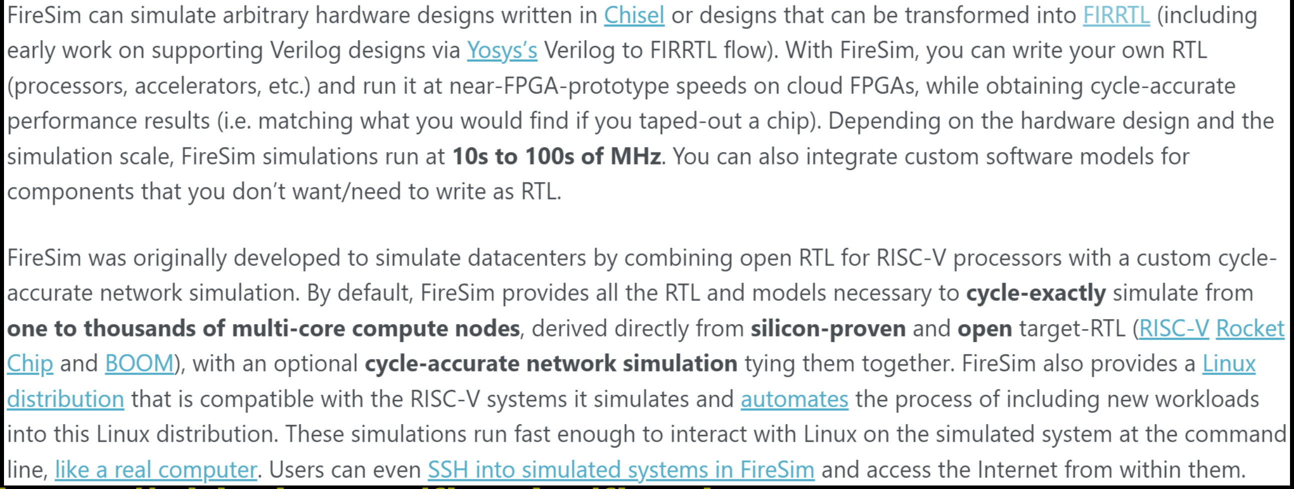
- https://fires.im/

Easy-to-use, FPGA-accelerated Cycle-accurate Hardware Simulation in the Cloud.



FireSim is an open-source cycle-accurate FPGA-accelerated full-system hardware simulation platform that runs on cloud FPGAs (Amazon EC2 F1). FireSim is actively developed in the Berkeley Architecture Research Group in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley.

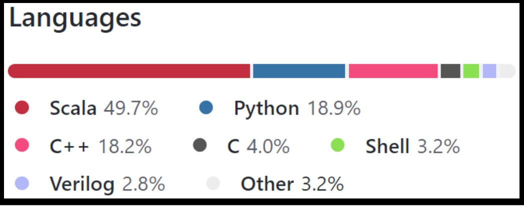
- **What can I simulate with FireSim?**



FireSim can simulate arbitrary hardware designs written in Chisel or designs that can be transformed into FIRRTL (including early work on supporting Verilog designs via Yosys's Verilog to FIRRTL flow). With FireSim, you can write your own RTL (processors, accelerators, etc.) and run it at near-FPGA-prototype speeds on cloud FPGAs, while obtaining cycle-accurate performance results (i.e. matching what you would find if you taped-out a chip). Depending on the hardware design and the simulation scale, FireSim simulations run at **10s to 100s of MHz**. You can also integrate custom software models for components that you don't want/need to write as RTL.

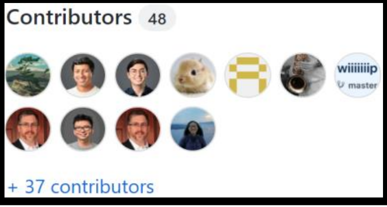
FireSim was originally developed to simulate datacenters by combining open RTL for RISC-V processors with a custom cycle-accurate network simulation. By default, FireSim provides all the RTL and models necessary to **cycle-exactly** simulate from **one to thousands of multi-core compute nodes**, derived directly from **silicon-proven** and **open** target-RTL (RISC-V Rocket Chip and BOOM), with an optional **cycle-accurate network simulation** tying them together. FireSim also provides a Linux distribution that is compatible with the RISC-V systems it simulates and automates the process of including new workloads into this Linux distribution. These simulations run fast enough to interact with Linux on the simulated system at the command line, like a real computer. Users can even SSH into simulated systems in FireSim and access the Internet from within them.

- https://github.com/firesim/firesim



Languages

● Scala 49.7% ● Python 18.9%
● C++ 18.2% ● C 4.0% ● Shell 3.2%
● Verilog 2.8% ● Other 3.2%



Contributors 48

+ 37 contributors

1.3.3 From RTL to CUDA

1.3.3.1 Overview

- https://research.nvidia.com/publication/2022-08_rtl-cuda-gpu-acceleration-flow-rtl-simulation-batch-stimulus

~~A GPU Acceleration Flow for RTL Simulation with Batch Stimulus.~~

- https://d1qx31qr3h6wln.cloudfront.net/publications/icpp22-rtlflow.pdf

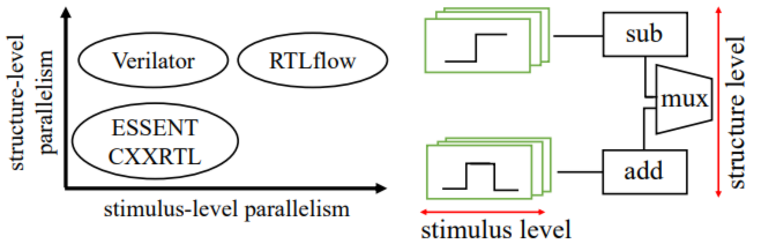
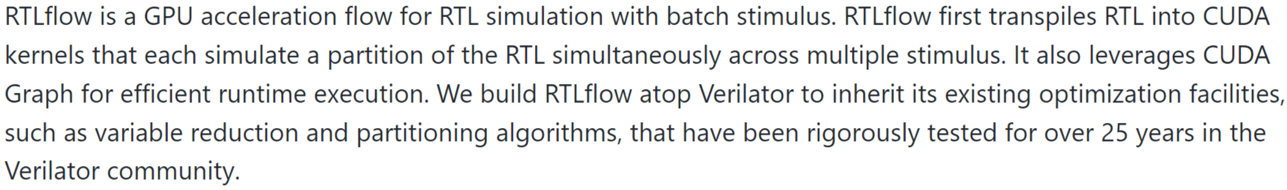
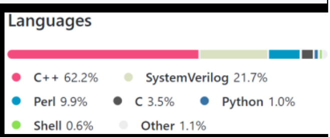


Figure 1: RTLflow explores both stimulus- and structure-level parallelisms to achieve high-performance RTL simulation using GPU computing.

- https://github.com/dian-lun-lin/RTLflow

forked from verilator/verilator


RTLflow is a GPU acceleration flow for RTL simulation with batch stimulus. RTLflow first transpiles RTL into CUDA kernels that each simulate a partition of the RTL simultaneously across multiple stimulus. It also leverages CUDA Graph for efficient runtime execution. We build RTLflow atop Verilator to inherit its existing optimization facilities, such as variable reduction and partitioning algorithms, that have been rigorously tested for over 25 years in the Verilator community.



- https://github.com/dian-lun-lin/RTLflow-benchmarks
- …

Workflow

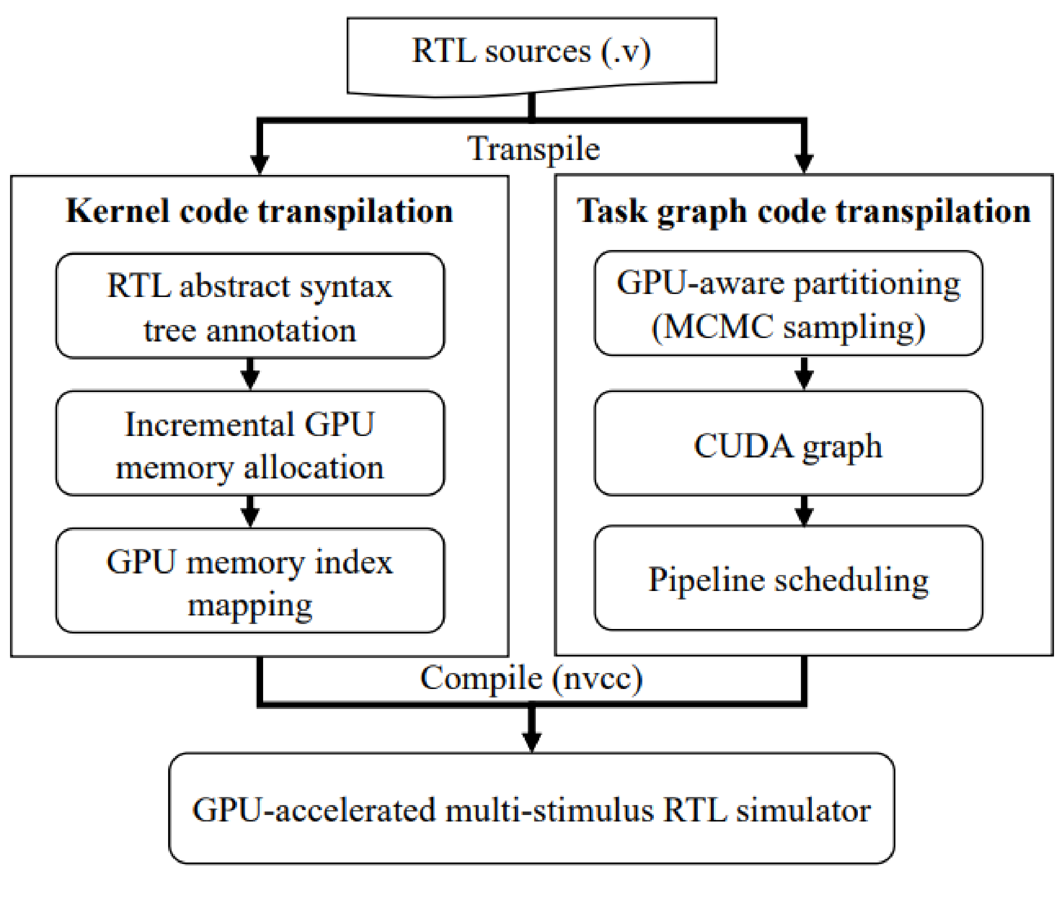

RTL sources (.v)
Transpile
Kernel code transpilation
RTL abstract syntax tree annotation
Incremental GPU memory allocation
GPU memory index mapping
Task graph code transpilation
GPU-aware partitioning (MCMC sampling)
CUDA graph
Pipeline scheduling
Compile (nvcc)
GPU-accelerated multi-stimulus RTL simulator

Figure 3: Overview of RTLflow.

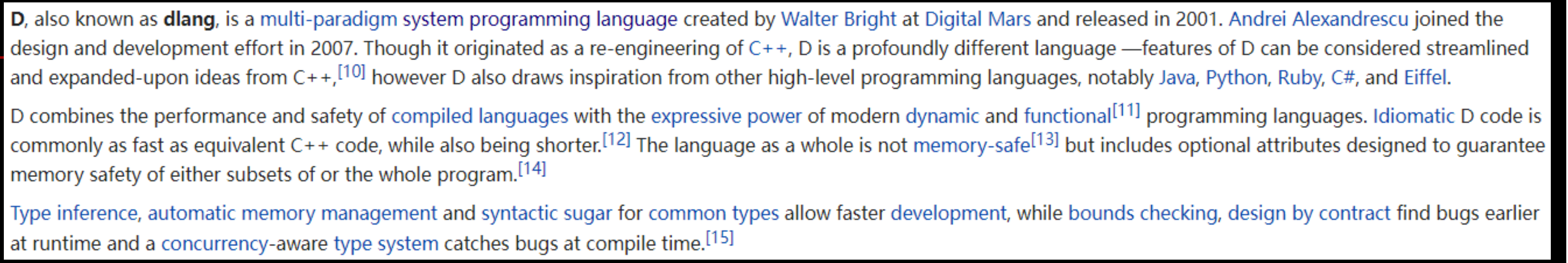
Source: https://d1qx31qr3h6wln.cloudfront.net/publications/icpp22-rtlflow.pdf

Python for Good
PyCon China 2022

2) Why is

2.1 Overview

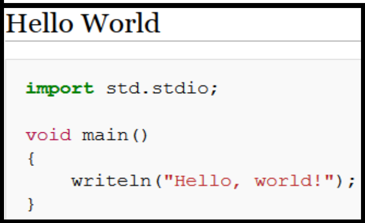
- https://en.wikipedia.org/wiki/D_(programming_language)



D, also known as **dlang**, is a multi-paradigm system programming language created by Walter Bright at Digital Mars and released in 2001. Andrei Alexandrescu joined the design and development effort in 2007. Though it originated as a re-engineering of C++, D is a profoundly different language —features of D can be considered streamlined and expanded-upon ideas from C++,[10] however D also draws inspiration from other high-level programming languages, notably Java, Python, Ruby, C#, and Eiffel.

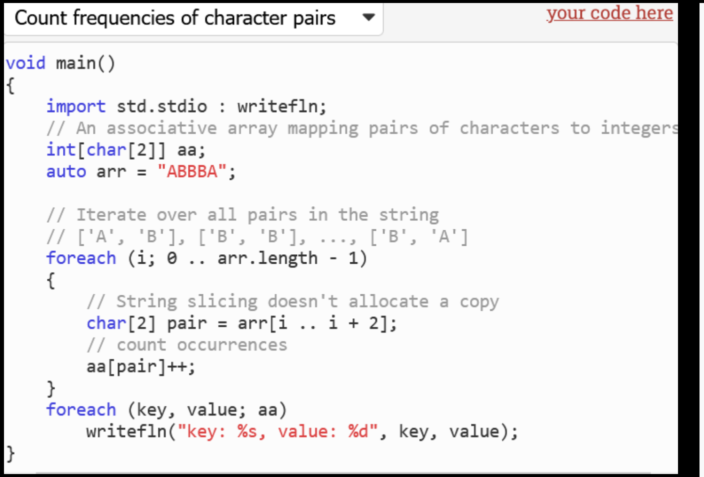
D combines the performance and safety of compiled languages with the expressive power of modern dynamic and functional[11] programming languages. Idiomatic D code is commonly as fast as equivalent C++ code, while also being shorter.[12] The language as a whole is not memory-safe[13] but includes optional attributes designed to guarantee memory safety of either subsets of or the whole program.[14]

Type inference, automatic memory management and syntactic sugar for common types allow faster development, while bounds checking, design by contract find bugs earlier at runtime and a concurrency-aware type system catches bugs at compile time.[15]



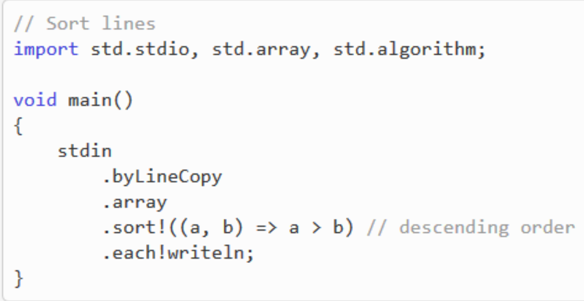
Hello World

```
import std.stdio;

void main()
{
    writeln("Hello, world!");
}
```

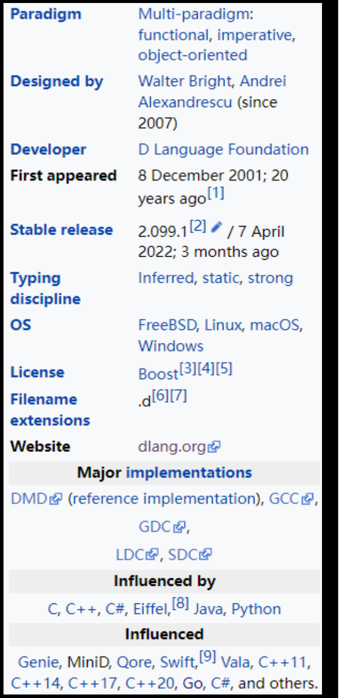


Count frequencies of character pairs ▼ your code here

```
void main()
{
    import std.stdio : writefln;
    // An associative array mapping pairs of characters to integers
    int[char[2]] aa;
    auto arr = "ABBBA";

    // Iterate over all pairs in the string
    // ['A', 'B'], ['B', 'B'], ..., ['B', 'A']
    foreach (i; 0 .. arr.length - 1)
    {
        // String slicing doesn't allocate a copy
        char[2] pair = arr[i .. i + 2];
        // count occurrences
        aa[pair]++;
    }
    foreach (key, value; aa)
        writefln("key: %s, value: %d", key, value);
}
```



```
// Sort lines
import std.stdio, std.array, std.algorithm;

void main()
{
    stdin
        .byLineCopy
        .array
        .sort!((a, b) => a > b) // descending order
        .each!writeln;
}
```

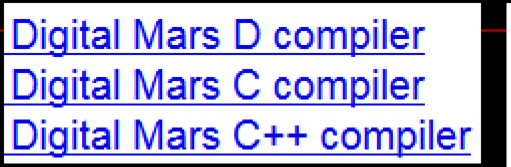


Paradigm	Multi-paradigm: functional, imperative, object-oriented
Designed by	Walter Bright, Andrei Alexandrescu (since 2007)
Developer	D Language Foundation
First appeared	8 December 2001; 20 years ago[1]
Stable release	2.099.1[2] / 7 April 2022; 3 months ago
Typing discipline	Inferred, static, strong
OS	FreeBSD, Linux, macOS, Windows
License	Boost[3][4][5]
Filename extensions	.d[6][7]
Website	dlang.org
Major implementations	
DMD (reference implementation), GCC, GDC, LDC, SDC	
Influenced by	
C, C++, C#, Eiffel,[8] Java, Python	
Influenced	
Genie, MiniD, Qore, Swift,[9] Vala, C++11, C++14, C++17, C++20, Go, C#, and others.	

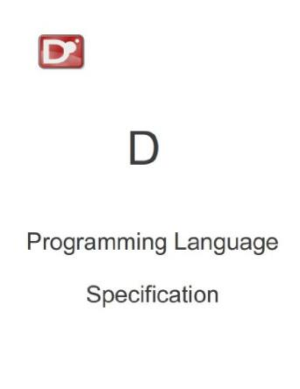
- https://dlang.org/spec/spec.html
- https://en.wikibooks.org/wiki/D_Programming
- ...

Designed by Experts

- https://en.wikipedia.org/wiki/D_(programming_language)
- https://en.wikipedia.org/wiki/Walter_Bright
  http://digitalmars.com/



Digital Mars D compiler
Digital Mars C compiler
Digital Mars C++ compiler

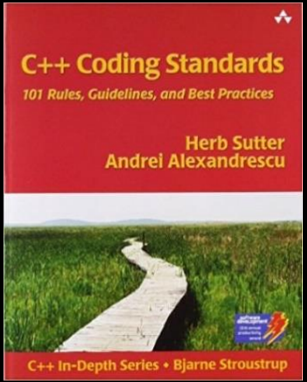


D

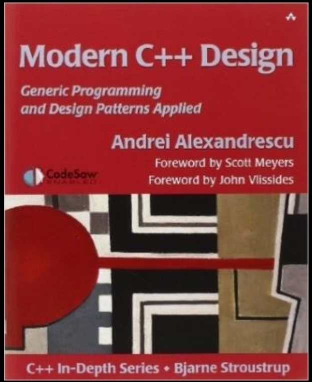
Programming Language

Specification

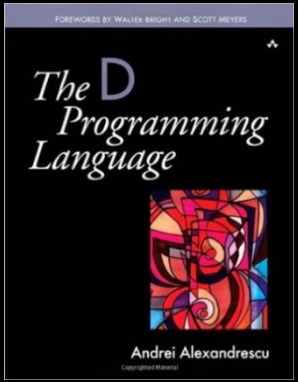
- https://en.wikipedia.org/wiki/Andrei_Alexandrescu
  http://erdani.org/



C++ Coding Standards
101 Rules, Guidelines, and Best Practices
Herb Sutter
Andrei Alexandrescu
C++ In-Depth Series • Bjarne Stroustrup



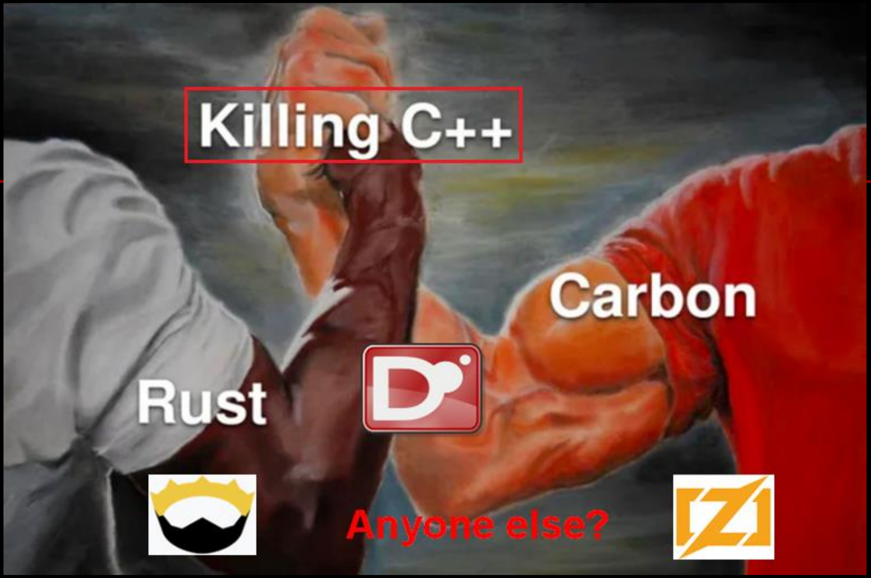
Modern C++ Design
Generic Programming and Design Patterns Applied
Andrei Alexandrescu
Foreword by Scott Meyers
Foreword by John Vlissides
C++ In-Depth Series • Bjarne Stroustrup



Forewords by Walter Bright and Scott Meyers
The D Programming Language
Andrei Alexandrescu

- Origins of the D Programming Language
  https://dl.acm.org/doi/abs/10.1145/3386323

I am here

- 

- **One idea: Why Modern Alternative Languages Never Replace C/C++**

  https://levelup.gitconnected.com/why-modern-alternative-languages-never- replace-c-c-cbf0afc5f1dc
- **But…**

If you are interested

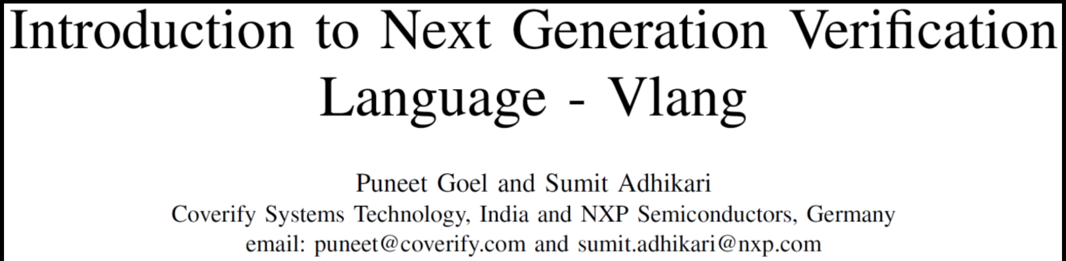
- For more materials, you may refer to our previous talks "Will D be a better system programming language" at OpenInfra Days China 2022(Online) and "First exploration of D for HW-SW co-designed system" at 1st OSEDA Workshop China 2022(Online).

3) Cocotb with D

3.1 Vlang

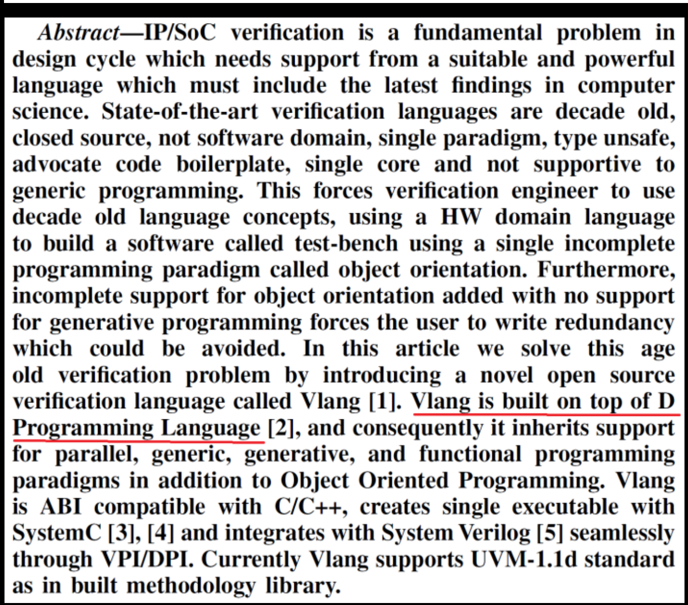
- A DSL built on top of D

Initial Design

- 

Introduction to Next Generation Verification Language - Vlang

Puneet Goel and Sumit Adhikari
Coverify Systems Technology, India and NXP Semiconductors, Germany
email: puneet@coverify.com and sumit.adhikari@nxp.com



Abstract—**IP/SoC verification is a fundamental problem in design cycle which needs support from a suitable and powerful language which must include the latest findings in computer science. State-of-the-art verification languages are decade old, closed source, not software domain, single paradigm, type unsafe, advocate code boilerplate, single core and not supportive to generic programming. This forces verification engineer to use decade old language concepts, using a HW domain language to build a software called test-bench using a single incomplete programming paradigm called object orientation. Furthermore, incomplete support for object orientation added with no support for generative programming forces the user to write redundancy which could be avoided. In this article we solve this age old verification problem by introducing a novel open source verification language called Vlang [1]. Vlang is built on top of D Programming Language [2], and consequently it inherits support for parallel, generic, generative, and functional programming paradigms in addition to Object Oriented Programming. Vlang is ABI compatible with C/C++, creates single executable with SystemC [3], [4] and integrates with System Verilog [5] seamlessly through VPI/DPI. Currently Vlang supports UVM-1.1d standard as in built methodology library.**

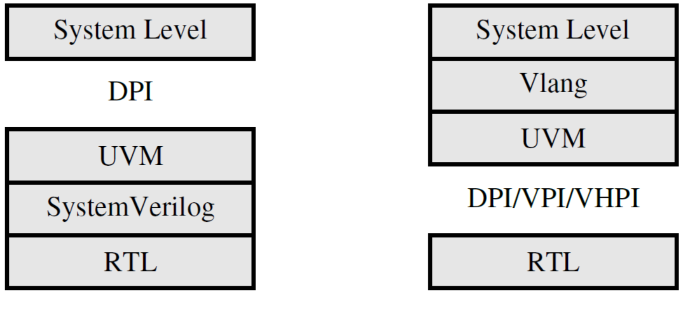
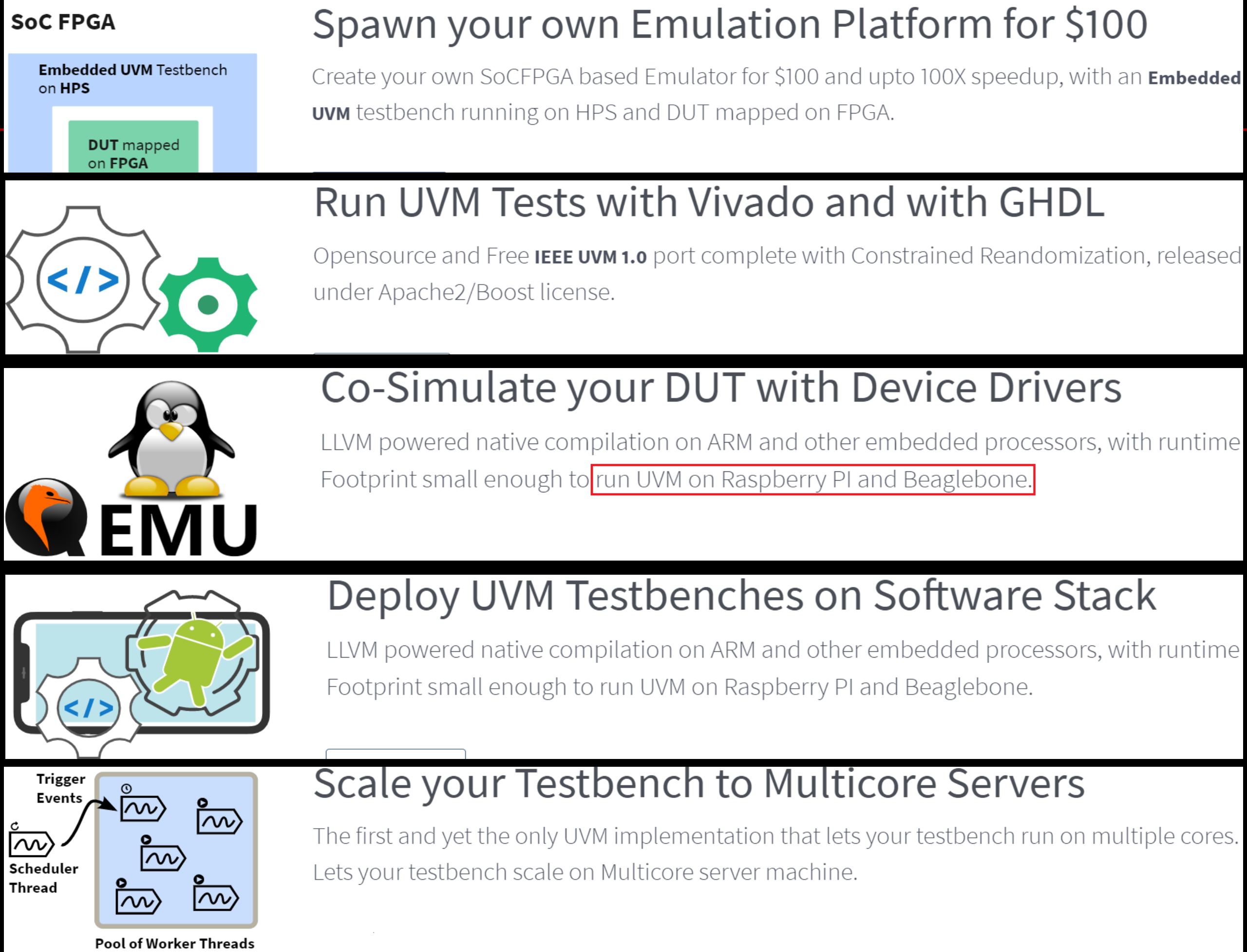


Fig. 1. Vlang vs System Verilog approach

Source: https://dvcon-proceedings.org/wp-content/uploads/introduction-to-next-generation-verification-language-vlang.pdf (DVCon Europe 2014)

3.1.1 Embedded UVM

- http://uvm.io/



Spawn your own Emulation Platform for $100

Create your own SoCFPGA based Emulator for $100 and upto 100X speedup, with an **Embedded UVM** testbench running on HPS and DUT mapped on FPGA.

Run UVM Tests with Vivado and with GHDL

Opensource and Free **IEEE UVM 1.0** port complete with Constrained Reandomization, released under Apache2/Boost license.

Co-Simulate your DUT with Device Drivers

LLVM powered native compilation on ARM and other embedded processors, with runtime Footprint small enough to run UVM on Raspberry PI and Beaglebone.

Deploy UVM Testbenches on Software Stack

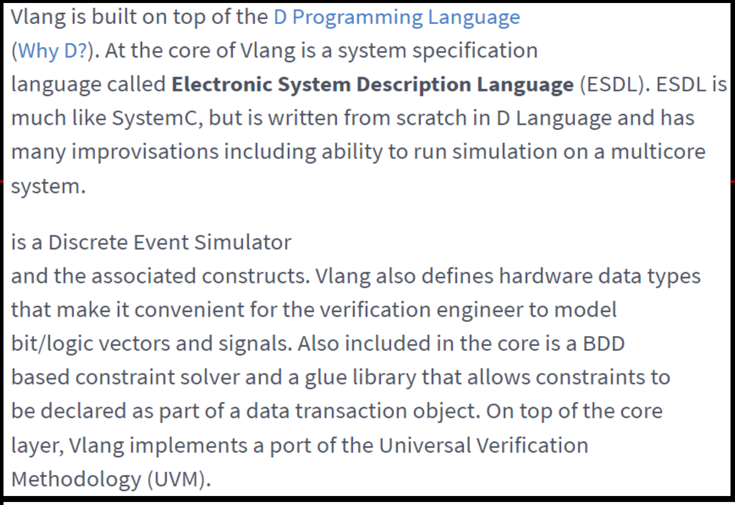
LLVM powered native compilation on ARM and other embedded processors, with runtime Footprint small enough to run UVM on Raspberry PI and Beaglebone.

Scale your Testbench to Multicore Servers

The first and yet the only UVM implementation that lets your testbench run on multiple cores. Lets your testbench scale on Multicore server machine.

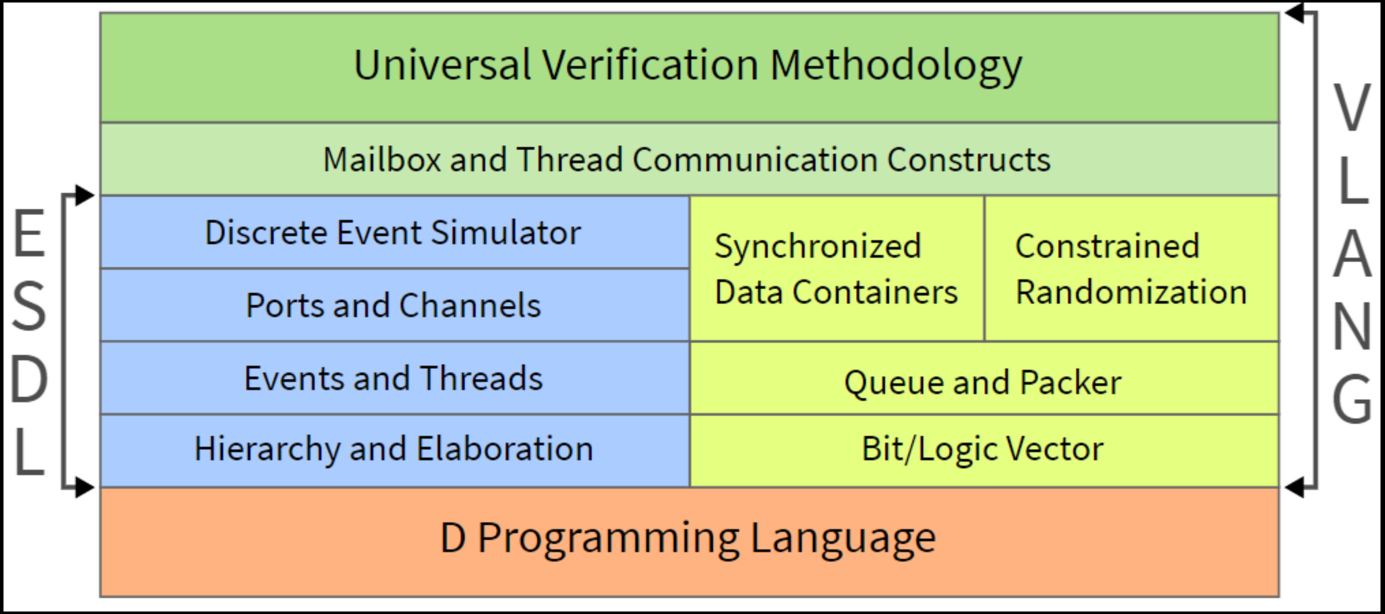
- Not production-ready, anyway, provides a good reference of design and code base for us.

Architecture & Design



Vlang is built on top of the D Programming Language (Why D?). At the core of Vlang is a system specification language called **Electronic System Description Language** (ESDL). ESDL is much like SystemC, but is written from scratch in D Language and has many improvisations including ability to run simulation on a multicore system.

is a Discrete Event Simulator and the associated constructs. Vlang also defines hardware data types that make it convenient for the verification engineer to model bit/logic vectors and signals. Also included in the core is a BDD based constraint solver and a glue library that allows constraints to be declared as part of a data transaction object. On top of the core layer, Vlang implements a port of the Universal Verification Methodology (UVM).



Universal Verification Methodology

Mailbox and Thread Communication Constructs

Discrete Event Simulator

Ports and Channels

Events and Threads

Hierarchy and Elaboration

Synchronized Data Containers

Constrained Randomization

Queue and Packer

Bit/Logic Vector

D Programming Language

ESDL

VLANG

Source: http://uvm.io/docs/core-concepts/architecture-overview/

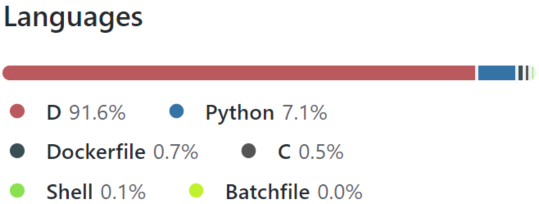
3.2 Replace C++ in Cocotb with D

- A long-term plan.
- If you are interested, you may look forward to our follow-ups such as "Revisiting D as a better system programming language", "Rethinking D for HW-SW co-designed system", and "Revisiting Cocotb as a Swiss Army Knife for hardware verification" in 2023…

3.2.1 PyD

3.2.1.1 Overview

- https://github.com/ariovistus/pyd
  Interoperability between Python and D.



Languages

● D 91.6% ● Python 7.1%
● Dockerfile 0.7% ● C 0.5%
● Shell 0.1% ● Batchfile 0.0%

Contributors 19

+ 8 contributors

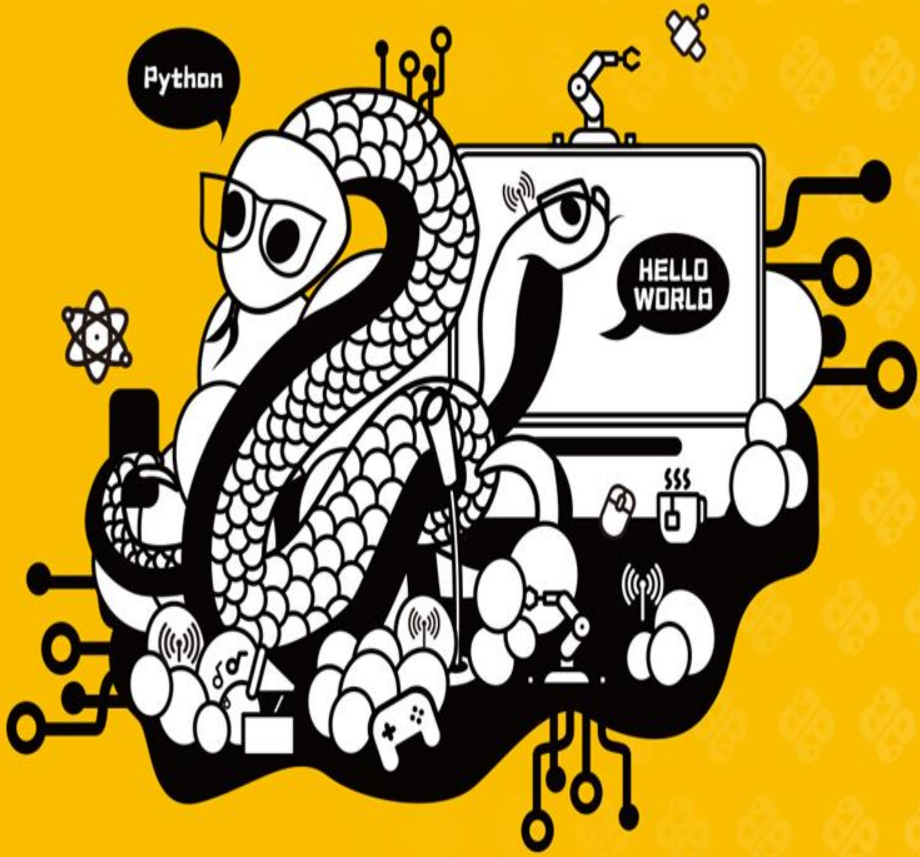
- …

The first thing is trying to add ARM and Python 3.11 support to PyD (currently only support X64).

V. Wrap-up

- A New Golden Age for Computer Architecture!
  A New Golden Age for Compiler Design!
  A New Golden Age for Programming Language and Runtime!
  A New Golden Age for FOSS EDA!
  A New Golden Age for HW-SW Co-design!

- Python plays a very important role in HW-SW Collaboration!



Thanks!

感谢观看

鲜卑拓跋枫

扫一扫上面的二维码图案，加我微信

Q & A

Reference

Slides/materials from many and varied sources:

- http://en.wikipedia.org/wiki/
- http://www.slideshare.net/
- https://en.wikipedia.org/wiki/SystemVerilog
- https://en.wikipedia.org/wiki/Device_under_test
- https://en.wikipedia.org/wiki/Coroutine
- https://buildmedia.readthedocs.org/media/pdf/pytest/latest/pytest.pdf
- https://docs.python-guide.org/writing/tests/
- https://qengineering.eu/install-vulkan-on-raspberry-pi.html
- https://semiengineering.com/knowledge_centers/eda-design /verification/hardware-assisted-verification/
- https://verificationacademy.com/verification-horizons/september-2021-volume-17-issue-2/hardware-assisted-verification-through-the-years
- https://www.chipestimate.com/EVEs-ZeBu-Hardware-Assisted-Verification-Platform-Used-by-Konica-Minolta-to-Implement-SystemVerilog-Assertions/Semiconductor-IP-Core/news/14555
- …